



LPC81xM

32-bit ARM Cortex-M0+ microcontroller; up to 16 kB flash and 4 kB SRAM

Rev. 1.0 — 7 November 2012

Objective data sheet

1. General description

The LPC81xM are an ARM Cortex-M0+ based, low-cost 32-bit MCU family operating at CPU frequencies of up to 30 MHz. The LPC81xM support up to 16 kB of flash memory and 4 kB of SRAM.

The peripheral complement of the LPC81xM includes a CRC engine, one I²C-bus interface, up to three USARTs, up to two SPI interfaces, one multi-rate timer, self wake-up timer, and state-configurable timer, one comparator, function-configurable I/O ports through a switch matrix, an input pattern match engine, and up to 18 general-purpose I/O pins.

2. Features and benefits

- System:
 - ◆ ARM Cortex-M0+ processor, running at frequencies of up to 30 MHz with single-cycle multiplier and fast single-cycle I/O port.
 - ◆ ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC).
 - ◆ System tick timer.
 - ◆ Serial Wire Debug (SWD) and JTAG boundary scan modes supported.
 - ◆ Micro Trace Buffer (MTB) supported.
- Memory:
 - ◆ 16 kB on-chip flash programming memory with 64 Byte page write and erase.
 - ◆ 4 kB SRAM.
- ROM API support:
 - ◆ Boot loader.
 - ◆ USART drivers.
 - ◆ I2C drivers.
 - ◆ Power profiles.
 - ◆ Flash In-Application Programming (IAP) and In-System Programming (ISP).
- Digital peripherals:
 - ◆ High-speed GPIO interface connected to the ARM Cortex-M0+ IO bus with up to 18 General-Purpose I/O (GPIO) pins with configurable pull-up/pull-down resistors.
 - ◆ GPIO interrupt generation capability with boolean pattern-matching feature on eight GPIO inputs.
 - ◆ Switch matrix for flexible configuration of each I/O pin function.
 - ◆ State Configurable Timer (SCT) with input and output functions (including capture and match) assigned to pins through the switch matrix.



- ◆ Multiple-channel multi-rate timer (MRT) for repetitive interrupt generation at up to four programmable, fixed rates.
- ◆ Self Wake-up Timer (WKT) clocked from either the IRC or a low-power, low-frequency internal oscillator.
- ◆ CRC engine.
- ◆ Windowed Watchdog timer (WWDT).
- Analog peripherals:
 - ◆ Comparator with external voltage reference with pin functions assigned or enabled through the switch matrix.
- Serial interfaces:
 - ◆ Three USART interfaces with pin functions assigned through the switch matrix.
 - ◆ Two SPI controllers with pin functions assigned through the switch matrix.
 - ◆ One I²C-bus interface with pin functions assigned through the switch matrix.
- Clock generation:
 - ◆ 12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
 - ◆ Crystal oscillator with an operating range of 1 MHz to 25 MHz.
 - ◆ Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
 - ◆ 10 kHz low-power oscillator for the WKT.
 - ◆ PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator, the external clock input CLKIN, or the internal RC oscillator.
 - ◆ Clock output function with divider that can reflect the crystal oscillator, the main clock, the IRC, or the watchdog oscillator.
- Power control:
 - ◆ Integrated PMU (Power Management Unit) to minimize power consumption.
 - ◆ Reduced power modes: Sleep mode, Deep-sleep mode, Power-down mode, and Deep power-down mode.
 - ◆ Power-On Reset (POR).
 - ◆ Brownout detect.
- Unique device serial number for identification.
- Single power supply.
- Available as SO20 package, TSSOP20 package, TSSOP16, and DIP8 package.

3. Applications

- | | |
|-------------------------|----------------------------------|
| ■ 8/16-bit applications | ■ Lighting |
| ■ Consumer | ■ Motor control |
| ■ Climate control | ■ Fire and security applications |

4. Ordering information

Table 1. Ordering information

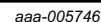
Type number	Package		
	Name	Description	Version
LPC810M021FN8	DIP8	plastic dual in-line package; 8 leads (300 mil)	SOT097-2
LPC811M001FDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101FDH16	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
LPC812M101FD20	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
LPC812M101FDH20	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1

4.1 Ordering options

Table 2. Ordering options

Type number	Flash/kB	SRAM/kB	USART	I ² C	SPI	Comparator	GPIO	Package
LPC810M021FN8	4	1	2	1	1	1	6	DIP8
LPC811M001FDH16	8	2	2	1	1	1	14	TSSOP16
LPC812M101FDH16	16	4	3	1	2	1	14	TSSOP16
LPC812M101FD20	16	4	2	1	1	1	18	SO20
LPC812M101FDH20	16	4	3	1	2	1	18	TSSOP20

LP001-M



6. Pinning information

6.1 Pinning

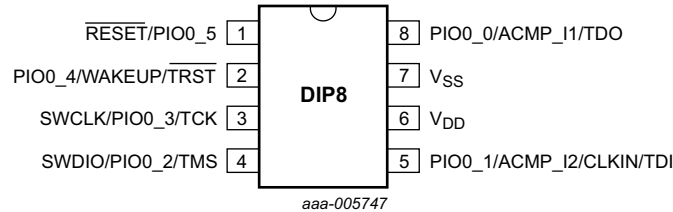


Fig 2. Pin configuration DIP8 package (LPC810M021FN8)

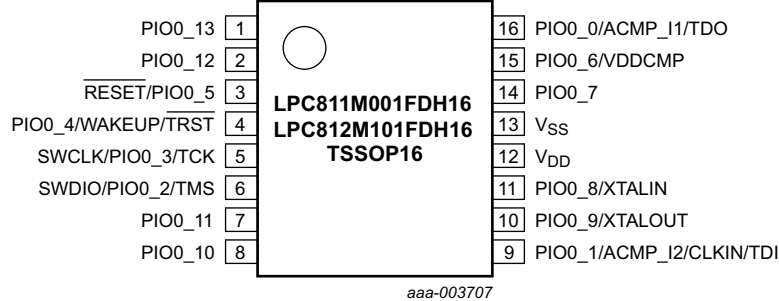


Fig 3. Pin configuration TSSOP16 package

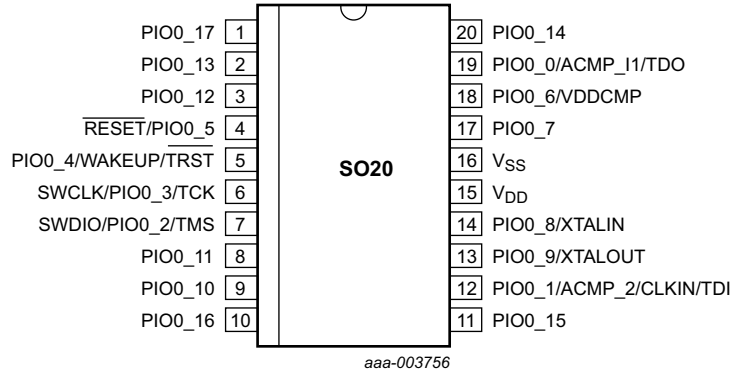


Fig 4. Pin configuration SO20 package (LPC812M101FD20)

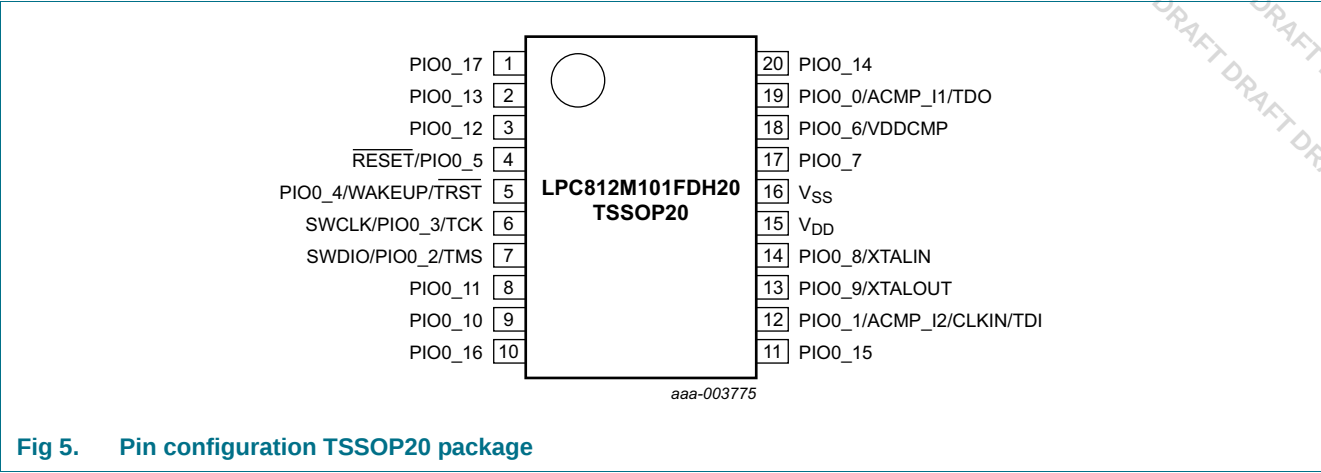


Fig 5. Pin configuration TSSOP20 package

6.2 Pin description

The pin description table [Table 3](#) shows the pin functions that are fixed to specific pins on each package. These fixed-pin functions are selectable between the GPIO, comparator, SWD, and the XTAL pins. By default, the GPIO function is selected except on pins PIO0_2, PIO0_3, and PIO0_5. JTAG functions are available in boundary scan mode only.

Movable function for the I2C, USART, SPI, and SCT pin functions can be assigned through the switch matrix to any pin that is not power or ground in place of the pin's fixed functions.

The following exceptions apply:

For full I2C-bus compatibility, assign the I2C functions to the open-drain pins PIO0_11 and PIO0_10.

Do not assign more than one output to any pin. However, more than one input can be assigned to a pin.

Pin PIO0_4 triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin.

The JTAG functions TDO, TDI, TCK, TMS, and $\overline{\text{TRST}}$ are selected on pins PIO0_0 to PIO0_4 by hardware when the part is in boundary scan mode.

Table 3. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	DIP8	Type	Reset state [1]	Description
PIO0_0/ACMP_I1/ TDO	19	16	8	[5] I/O	I; PU	PIO0_0 — General purpose digital input/output port 0 pin 0. In ISP mode, this is the USART0 receive pin U0_RXD. In boundary scan mode: TDO (Test Data Out).
				AI	-	ACMP_I1 — Analog comparator input 1.
PIO0_1/ACMP_I2/ CLKIN/TDI	12	9	5	[5] I/O	I; PU	PIO0_1 — General purpose digital input/output pin. ISP entry pin. A LOW level on this pin during reset starts the ISP command handler. In boundary scan mode: TDI (Test Data In).
				AI	-	ACMP_I2 — Analog comparator input 2.
				I	-	CLKIN — External clock input.
SWDIO/PIO0_2/TMS	7	6	4	[2] I/O	I; PU	SWDIO — Serial Wire Debug I/O. SWDIO is enabled by default on this pin. In boundary scan mode: TMS (Test Mode Select).
				I/O	-	PIO0_2 — General purpose digital input/output pin.
SWCLK/PIO0_3/ TCK	6	5	3	[2] I/O	I; PU	SWCLK — Serial Wire Clock. SWCLK is enabled by default on this pin. In boundary scan mode: TCK (Test Clock).
				I/O	-	PIO0_3 — General purpose digital input/output pin.

Table 3. Pin description table (fixed pins)

Symbol	SO20/ TSSOP20	TSSOP16	DIP8	Type	Reset state [1]	Description
$\overline{\text{PIO0_4}}$ /WAKEUP/ $\overline{\text{TRST}}$	5	4	2	[6] I/O	I; PU	PIO0_4 — General purpose digital input/output pin. In ISP mode, this is the USART0 transmit pin U0_TXD. In boundary scan mode: $\overline{\text{TRST}}$ (Test Reset). This pin triggers a wake-up from Deep power-down mode. If you need to wake up from Deep power-down mode via an external pin, do not assign any movable function to this pin. Pull this pin HIGH externally to enter Deep power-down mode. Pull this pin LOW to exit Deep power-down mode. A LOW-going pulse as short as 50 ns wakes up the part.
$\overline{\text{RESET}}$ /PIO0_5	4	3	1	[4] I/O	I; PU	RESET — External reset input: A LOW-going pulse as short as 50 ns on this pin resets the device, causing I/O ports and peripherals to take on their default states, and processor execution to begin at address 0.
				I	-	PIO0_5 — General purpose digital input/output pin.
PIO0_6/VDDCMP	18	15	-	[9] I/O	I; PU	PIO0_6 — General purpose digital input/output pin.
				AI	-	VDDCMP — Alternate reference voltage for the analog comparator.
PIO0_7	17	14	-	[2] I/O	I; PU	PIO0_7 — General purpose digital input/output pin.
PIO0_8/XTALIN	14	11	-	[8] I/O	I; PU	PIO0_8 — General purpose digital input/output pin.
				I	-	XTALIN — Input to the oscillator circuit and internal clock generator circuits. Input voltage must not exceed 1.95 V.
PIO0_9/XTALOUT	13	10	-	[8] I/O	I; PU	PIO0_9 — General purpose digital input/output pin.
				O	-	XTALOUT — Output from the oscillator circuit.
PIO0_10	9	8	-	[3] I	IA	PIO0_10 — General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_11	8	7	-	[3] I	IA	PIO0_11 — General purpose digital input/output pin. Assign I2C functions to this pin when true open-drain pins are needed for a signal compliant with the full I2C specification.
PIO0_12	3	2	-	[2] I/O	I; PU	PIO0_12 — General purpose digital input/output pin.
PIO0_13	2	1	-	[2] I/O	I; PU	PIO0_13 — General purpose digital input/output pin.
PIO0_14	20	-	-	[7] I/O	I; PU	PIO0_14 — General purpose digital input/output pin.
PIO0_15	11	-	-	[7] I/O	I; PU	PIO0_15 — General purpose digital input/output pin.
PIO0_16	10	-	-	[7] I/O	I; PU	PIO0_16 — General purpose digital input/output pin.
PIO0_17	1	-	-	[7] I/O	I; PU	PIO0_17 — General purpose digital input/output pin.
V _{DD}	15	12	6	-	-	3.3 V supply voltage.
V _{SS}	16	13	7	-	-	Ground.

[1] Pin state at reset for default function: I = Input; AI = Analog Input; O = Output; PU = internal pull-up enabled (pins pulled up to full V_{DD} level); IA = inactive, no pull-up/down enabled.

[2] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis; includes high-current output driver.

[3] True open-drain pin. I²C-bus pins compliant with the I²C-bus specification for I²C standard mode, I²C Fast-mode, and I²C Fast-mode Plus. Do not use this pad for high-speed applications such as SPI or USART.

- [4] See [Figure 10](#) for the reset pad configuration. $\overline{\text{RESET}}$ functionality is not available in Deep power-down mode. Use the WAKEUP pin to reset the chip and wake up from Deep power-down mode. An external pull-up resistor is required on this pin for the Deep power-down mode.
- [5] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog input. When configured as an analog input, the digital section of the pin is disabled, and the pin is not 5 V tolerant.
- [6] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis. In Deep power-down mode, pulling this pin LOW wakes up the chip.
- [7] 5 V tolerant pad providing digital I/O functions with configurable pull-up/pull-down resistors and configurable hysteresis.
- [8] 5 V tolerant pin providing standard digital I/O functions with configurable modes, configurable hysteresis, and analog I/O for the system oscillator. When configured as an analog I/O, the digital section of the pin is disabled, and the pin is not 5 V tolerant.
- [9] The digital part of this pin is 3 V tolerant pin due to special analog functionality. Pin provides standard digital I/O functions with configurable modes, configurable hysteresis, and an analog input. When configured as an analog input, the digital section of the pin is disabled.

Table 4. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
U0_TXD	O	Transmitter output for USART0.
U0_RXD	I	Receiver input for USART0.
U0_RTS	O	Request To Send output for USART0.
U0_CTS	I	Clear To Send input for USART0.
U0_SCLK	I/O	Serial clock input/output for USART0 in synchronous mode.
U1_TXD	O	Transmitter output for USART1.
U1_RXD	I	Receiver input for USART1.
U1_RTS	O	Request To Send output for USART1.
U1_CTS	I	Clear To Send input for USART1.
U1_SCLK	I/O	Serial clock input/output for USART1 in synchronous mode.
U2_TXD	O	Transmitter output for USART2.
U2_RXD	I	Receiver input for USART2.
U2_RTS	O	Request To Send output for USART2.
U2_CTS	I	Clear To Send input for USART2.
U2_SCLK	I/O	Serial clock input/output for USART2 in synchronous mode.
SPI0_SCK	I/O	Serial clock for SPI0.
SPI0_MOSI	I/O	Master Out Slave In for SPI0.
SPI0_MISO	I/O	Master In Slave Out for SPI0.
SPI0_SSEL	I/O	Slave select for SPI0.
SPI1_SCK	I/O	Serial clock for SPI1.
SPI1_MOSI	I/O	Master Out Slave In for SPI1.
SPI1_MISO	I/O	Master In Slave Out for SPI1.
SPI1_SSEL	I/O	Slave select for SPI1.
CTIN_0	I	SCT input 0.
CTIN_1	I	SCT input 1.
CTIN_2	I	SCT input 2.
CTIN_3	I	SCT input 3.
CTOUT_0	O	SCT output 0.
CTOUT_1	O	SCT output 1.
CTOUT_2	O	SCT output 2.

Table 4. Movable functions (assign to pins PIO0_0 to PIO_17 through switch matrix)

Function name	Type	Description
CTOUT_3	O	SCT output 3.
I2C0_SCL	I/O	I ² C-bus clock input/output (open-drain if assigned to pin PIO0_10). High-current sink only if assigned to PIO0_10 and if I ² C Fast-mode Plus is selected in the I/O configuration register.
I2C0_SDA	I/O	I ² C-bus data input/output (open-drain if assigned to pin PIO0_11). High-current sink only if assigned to pin PIO0_11 and if I ² C Fast-mode Plus is selected in the I/O configuration register.
ACMP_O	O	Analog comparator output.
CLKOUT	O	Clock output.
GPIO_INT_BMAT	O	Output of the pattern match engine.

7. Functional description

7.1 ARM Cortex-M0+ core

The ARM Cortex-M0+ core runs at an operating frequency of up to 30 MHz using a two-stage pipeline. Integrated in the core are the NVIC and Serial Wire Debug with four breakpoints and two watchpoints. The ARM Cortex-M0+ core supports a single-cycle I/O enabled port for fast GPIO access.

The core includes a single-cycle multiplier and a system tick timer.

7.2 On-chip flash program memory

The LPC81xM contain up to 16 kB of on-chip flash program memory. The flash memory supports a 64 Byte page size with page write and erase.

7.3 On-chip SRAM

The LPC81xM contain a total of 1 kB, 2 kB, or 4 kB on-chip static RAM data memory.

7.4 On-chip ROM

The 8 kB on-chip ROM contains the boot loader and the following Application Programming Interfaces (API):

- In-System Programming (ISP) and In-Application Programming (IAP) support for flash programming
- Power profiles for configuring power consumption and PLL settings
- USART driver API routines
- I²C-bus driver API routines

7.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is an integral part of the Cortex-M0+. The tight coupling to the CPU allows for low interrupt latency and efficient processing of late arriving interrupts.

7.5.1 Features

- Controls system exceptions and peripheral interrupts.
- In the LPC81xM, the NVIC supports 32 vectored interrupts including up to 8 external interrupt inputs selectable from all GPIO pins.
- Four programmable interrupt priority levels with hardware priority level masking.
- Software interrupt generation using the ARM exceptions SVCALL and PENDSV.
- Relocatable interrupt vector table.

7.5.2 Interrupt sources

Each peripheral device has one interrupt line connected to the NVIC but may have several interrupt flags. Individual interrupt flags may also represent more than one interrupt source.

Up to eight pins, regardless of the selected function, can be programmed to generate an interrupt on a level, a rising or falling edge, or both. The interrupt generating pins can be selected from all digital or mixed digital/analog pins. The pin interrupt/pattern match block controls the edge or level detection mechanism.

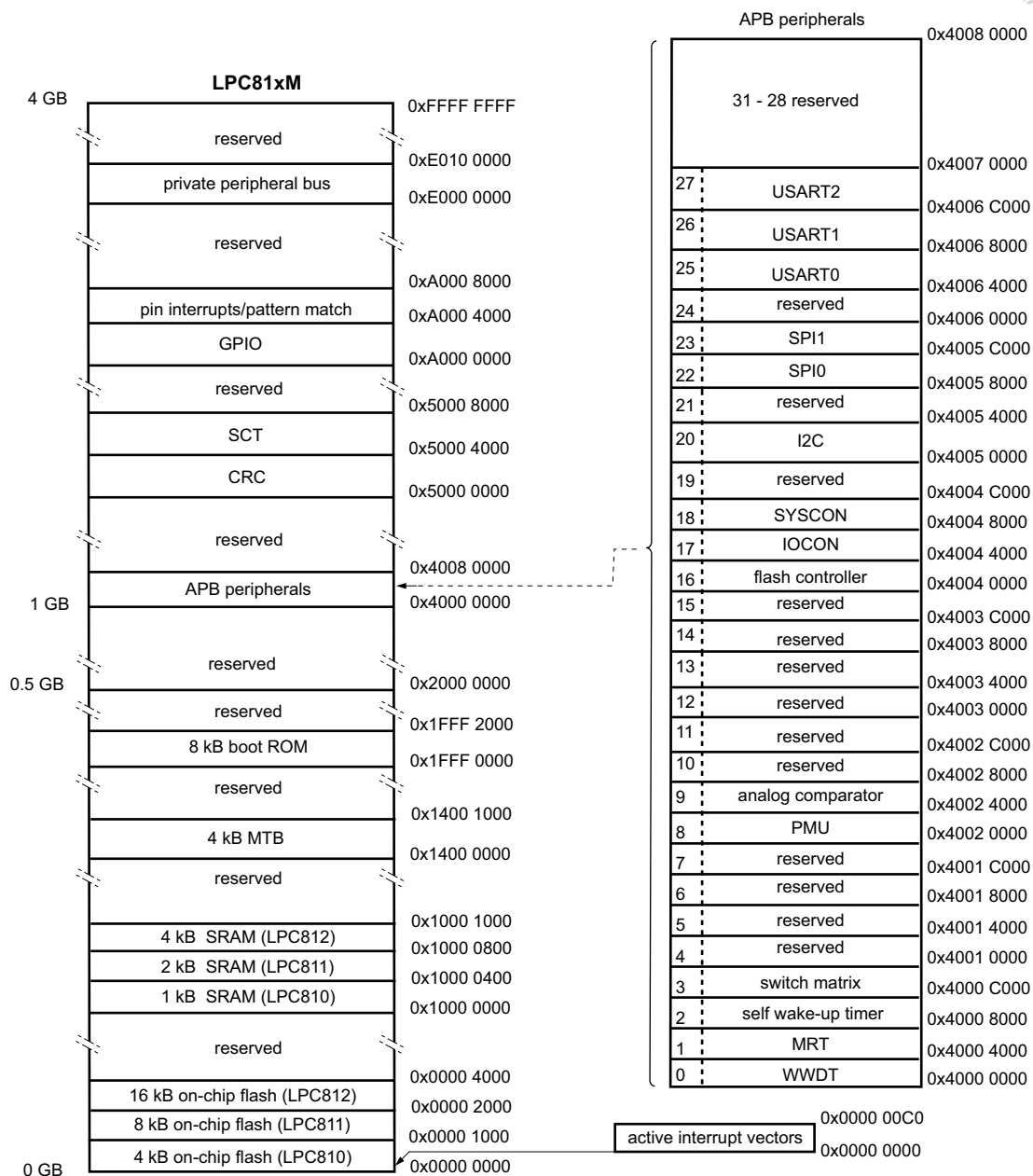
7.6 System tick timer

The ARM Cortex-M0+ includes a 24-bit system tick timer (SysTick) that is intended to generate a dedicated SysTick exception at a fixed time interval (typically 10 ms).

7.7 Memory map

The LPC81xM incorporates several distinct memory regions. [Figure 6](#) shows the overall map of the entire address space from the user program viewpoint following reset. The interrupt vector area supports address remapping.

The ARM private peripheral bus includes the ARM core registers for controlling the NVIC, the system tick timer (SysTick), and the reduced power modes.



aaa-005748

Fig 6. LPC81xM Memory map

7.8 I/O configuration

The IOCON block controls the configuration of the I/O pins. Each digital or mixed digital/analog pin with the PIO0_n designator (except the true open-drain pins PIO0_10 and PIO0_11) in [Table 3](#) can be configured as follows:

- Enable or disable the weak internal pull-up and pull-down resistors.
- Select a pseudo open-drain mode. The input cannot be pulled up above V_{DD} .

- Program the input glitch filter with different filter constants using one of the IOCON divided clock signals (IOCONCLKCDIV, see [Figure 9 “LPC81xM clock generation”](#)). You can also bypass the glitch filter.
- Invert the input signal.
- Hysteresis can be enabled or disabled.
- For pins PIO0_10 and PIO0_11, select the I2C-mode and output driver for standard digital operation, for I2C standard and fast modes, or for I2C Fast mode+.
- On mixed digital/analog pins, enable the analog input mode. Enabling the analog mode disconnects the digital functionality.

Remark: The functionality of each I/O pin is flexible and is determined entirely through the switch matrix. See [Section 7.9](#) for details.

7.8.1 Standard I/O pad configuration

[Figure 7](#) shows the possible pin modes for standard I/O pins with analog input function:

- Digital output driver with configurable open-drain output
- Digital input: Weak pull-up resistor (PMOS device) enabled/disabled
- Digital input: Weak pull-down resistor (NMOS device) enabled/disabled
- Digital input: Repeater mode enabled/disabled
- Digital input: Input glitch filter selectable on all pins
- Analog input

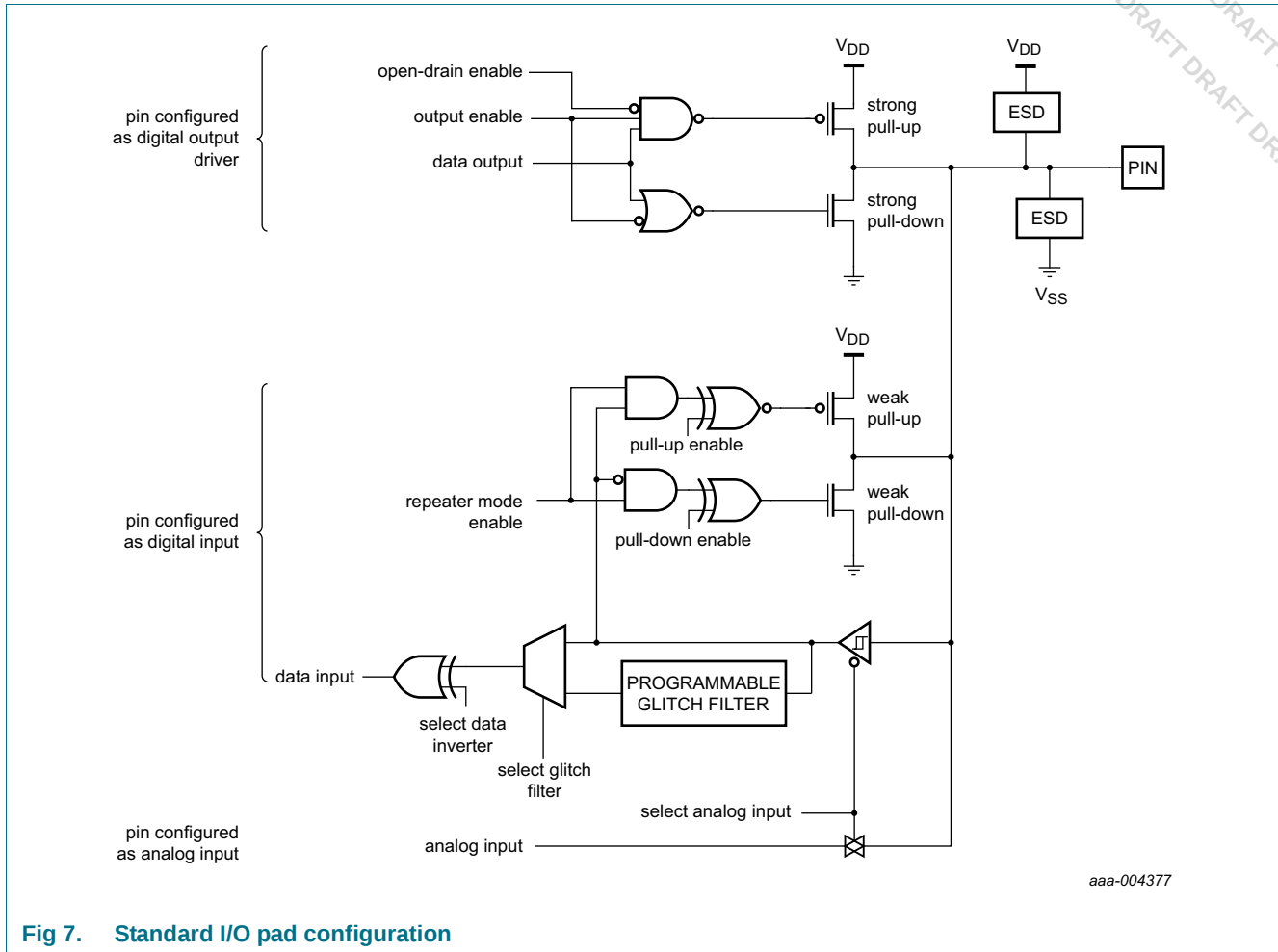


Fig 7. Standard I/O pad configuration

7.9 Switch Matrix (SWM)

The switch matrix controls the function of each digital or mixed analog/digital pin in a highly flexible way by allowing to connect many functions like the USART, SPI, SCT, and I2C functions to any pin that is not power or ground. These functions are called movable functions and are listed in [Table 4](#).

Functions that need specialized pads like the oscillator pins XTALIN and XTALOUT can be enabled or disabled through the switch matrix. These functions are called fixed-pin functions and cannot move to other pins. The fixed-pin functions are listed in [Table 3](#). If a fixed-pin function is disabled, any other movable function can be assigned to this pin.

7.10 Fast General-Purpose parallel I/O (GPIO)

Device pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC81xM use accelerated GPIO functions:

- GPIO registers are located on the ARM Cortex M0+ IO bus for fastest possible single-cycle I/O timing.

- An entire port value can be written in one instruction.
- Mask, set, and clear operations are supported for the entire port.

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin. Except for pins SWDIO/PIO0_2, SWCLK/PIO0_3, and RESET/PIO0_5, the switch matrix enables the GPIO port pin function by default.

7.10.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation.
- Direction control of individual bits.
- All I/O default to inputs with internal pull-up resistors enabled after reset - except for the I²C-bus true open-drain pins PIO0_2 and PIO0_3.
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin (see [Figure 7](#)).
- Control of the digital output slew rate allowing to switch more outputs simultaneously without degrading the power/ground distribution of the device.

7.11 Pin interrupt/pattern match engine

The pin interrupt block configures up to eight pins from all digital pins for providing eight external interrupts connected to the NVIC.

The pattern match engine can be used, in conjunction with software, to create complex state machines based on pin inputs.

Any digital pin, independently of the function selected through the switch matrix, can be configured through the SYSCON block as input to the pin interrupt or pattern match engine. The registers that control the pin interrupt or pattern match engine are located on the IO+ bus for fast single-cycle access.

7.11.1 Features

- Pin interrupts
 - Up to eight pins can be selected from all digital pins as edge- or level-sensitive interrupt requests. Each request creates a separate interrupt in the NVIC.
 - Edge-sensitive interrupt pins can interrupt on rising or falling edges or both.
 - Level-sensitive interrupt pins can be HIGH- or LOW-active.
 - Pin interrupts can wake up the LPC81xM from sleep mode, deep-sleep mode, and deep power-down mode.
- Pin interrupt pattern match engine
 - Up to 8 pins can be selected from all digital pins to contribute to a boolean expression. The boolean expression consists of specified levels and/or transitions on various combinations of these pins.
 - Each minterm (product term) comprising the specified boolean expression can generate its own, dedicated interrupt request.

- Any occurrence of a pattern match can be programmed to also generate an RXEV notification to the ARM CPU. The RXEV signal can be connected to a pin.
- The pattern match engine does not facilitate wake-up.

7.12 USART0/1/2

Remark: USART0 and USART1 are available on all LPC800 parts. USART2 is available on parts LPC812M101FDH16 and LPC812M101FDH20 only.

All USART functions are movable functions and are assigned to pins through the switch matrix.

7.12.1 Features

- Maximum bit rates of 1.875 Mbit/s in asynchronous mode and 30 Mbit/s in synchronous mode for USART functions connected to all digital pins except PIO0_10 and PIO0_11.
- 7, 8, or 9 data bits and 1 or 2 stop bits
- Synchronous mode with master or slave operation. Includes data phase selection and continuous clock option.
- Multiprocessor/multidrop (9-bit) mode with software address compare. (RS-485 possible with software address detection and transceiver direction control.)
- Parity generation and checking: odd, even, or none.
- One transmit and one receive data buffer.
- RTS/CTS for hardware signaling for automatic flow control. Software flow control can be performed using Delta CTS detect, Transmit Disable control, and any GPIO as an RTS output.
- Received data and status can optionally be read from a single register
- Break generation and detection.
- Receive data is 2 of 3 sample "voting". Status flag set when one sample differs.
- Built-in Baud Rate Generator.
- A fractional rate divider is shared among all UARTs.
- Interrupts available for Receiver Ready, Transmitter Ready, Receiver Idle, change in receiver break detect, Framing error, Parity error, Overrun, Underrun, Delta CTS detect, and receiver sample noise detected.
- Separate data and flow control loopback modes for testing.
- Baud rate clock can also be output in asynchronous mode.
- Supported by on-chip ROM API.

7.13 SPI0/1

Remark: SPI0 is available on all LPC800 parts. SPI1 is available on parts LPC812M101FDH16 and LPC812M101FDH20 only.

All SPI functions are movable functions and are assigned to pins through the switch matrix.

7.13.1 Features

- Maximum data rates of 30 Mbit/s in slave and master mode for SPI functions connected to all digital pins except PIO0_10 and PIO0_11.
- Data frames of 1 to 16 bits supported directly. Larger frames supported by software.
- Master and slave operation.
- Data can be transmitted to a slave without the need to read incoming data. This can be useful while setting up an SPI memory.
- Control information can optionally be written along with data. This allows very versatile operation, including “any length” frames.
- One Slave Select input/output with selectable polarity and flexible usage.

Remark: Texas Instruments SSI and National Microwire modes are not supported.

7.14 I2C-bus interface

The I²C-bus is bidirectional for inter-IC control using only two wires: a serial clock line (SCL) and a serial data line (SDA). Each device is recognized by a unique address and can operate as either a receiver-only device (e.g., an LCD driver) or a transmitter with the capability to both receive and send information (such as memory). Transmitters and/or receivers can operate in either master or slave mode, depending on whether the chip has to initiate a data transfer or is only addressed. The I²C is a multi-master bus and can be controlled by more than one bus master connected to it.

The I2C-bus functions are movable functions and can be assigned through the switch matrix to any pin. However, only the true open-drain PIO0_10 and PIO0_11 provide the electrical characteristics to support the full I2C-bus specification (see [Ref. 1](#)).

7.14.1 Features

- Supports standard and fast mode with data rates of up to 400 kbit/s.
- Independent Master, Slave, and Monitor functions.
- Supports both Multi-master and Multi-master with Slave functions.
- Multiple I²C slave addresses supported in hardware.
- One slave address can be selectively qualified with a bit mask or an address range in order to respond to multiple I²C bus addresses.
- 10-bit addressing supported with software assist.
- Supports SMBus.
- Supported by on-chip ROM API.
- If the I2C functions are connected to the true open-drain pins (PIO0_10 and PIO0_11), the I2C supports the full I2C-bus specification:
 - Fail-safe operation: When the power to an I²C-bus device is switched off, the SDA and SCL pins connected to the I²C-bus are floating and do not disturb the bus.
 - Supports Fast-mode Plus with bit rates up to 1 Mbit/s.

7.15 State-Configurable Timer (SCT)

The state configurable timer can perform basic 16-bit and 32-bit timer/counter functions with match outputs and external and internal capture inputs. In addition, the SCT can employ up to two different programmable states, which can change under the control of events, to provide complex timing patterns.

All inputs and outputs of the SCT are movable functions and are assigned to pins through the switch matrix.

7.15.1 Features

- Two 16-bit counters or one 32-bit counter.
- Counters clocked by bus clock or selected input.
- Up counters or up-down counters.
- State variable allows sequencing across multiple counter cycles.
- The following conditions define an event: a counter match condition, an input (or output) condition, a combination of a match and/or input/output condition in a specified state, and the count direction.
- Events control outputs, interrupts, and the SCT states.
 - Match register 0 can be used as an automatic limit.
 - In bi-directional mode, events can be enabled based on the count direction.
 - Match events can be held until another qualifying event occurs.
- Selected events can limit, halt, start, or stop a counter.
- Supports:
 - 4 inputs
 - 4 outputs
 - 5 match/capture registers
 - 6 events
 - 2 states

7.16 Multi-Rate Timer (MRT)

The Multi-Rate Timer (MRT) provides a repetitive interrupt timer with four channels. Each channel can be programmed with an independent time interval, and each channel operates independently from the other channels.

7.16.1 Features

- 24-bit interrupt timer
- Four channels independently counting down from individually set values
- Repeat and one-shot interrupt modes

7.17 Windowed WatchDog Timer (WWDT)

The watchdog timer resets the controller if software fails to periodically service it within a programmable time window.

7.17.1 Features

- Internally resets chip if not periodically reloaded during the programmable time-out period.
- Optional windowed operation requires reload to occur between a minimum and maximum time period, both programmable.
- Optional warning interrupt can be generated at a programmable time prior to watchdog time-out.
- Enabled by software but requires a hardware reset or a watchdog reset/interrupt to be disabled.
- Incorrect feed sequence causes reset or interrupt if enabled.
- Flag to indicate watchdog reset.
- Programmable 24-bit timer with internal prescaler.
- Selectable time period from $(T_{cy(WDCLK)} \times 256 \times 4)$ to $(T_{cy(WDCLK)} \times 2^{24} \times 4)$ in multiples of $T_{cy(WDCLK)} \times 4$.
- The Watchdog Clock (WDCLK) source can be selected from the internal RC oscillator (IRC), or the dedicated watchdog oscillator (WDOsc). This gives a wide range of potential timing choices of watchdog operation under different power conditions.

7.18 Self Wake-up Timer (WKT)

The self wake-up timer is a 32-bit, loadable down-counter. Writing any non-zero value to this timer automatically enables the counter and launches a count-down sequence. When the counter is used as a wake-up timer, this write can occur just prior to entering a reduced power mode.

7.18.1 Features

- 32-bit loadable down-counter. Counter starts automatically when a count value is loaded. Time-out generates an interrupt/wake up request.
- The WKT resides in a separate, always-on power domain.
- The WKT supports two clock sources. One clock source originates from the always-on power domain.
- The WKT can be used for waking up the part from any reduced power mode, including Deep power-down mode, or for general-purpose timing.

7.19 Analog comparator (ACMP)

The analog comparator with selectable hysteresis can compare voltage levels on external pins and internal voltages.

After power-up and after switching the input channels of the comparator, the output of the voltage ladder must be allowed to settle to its stable value before it can be used as a comparator reference input. Settling times are given in [Table 23](#).

The analog comparator output is a movable function and is assigned to a pin through the switch matrix. The comparator inputs and the voltage reference are enabled or disabled on pins PIO0_0 and PIO0_1 through the switch matrix.

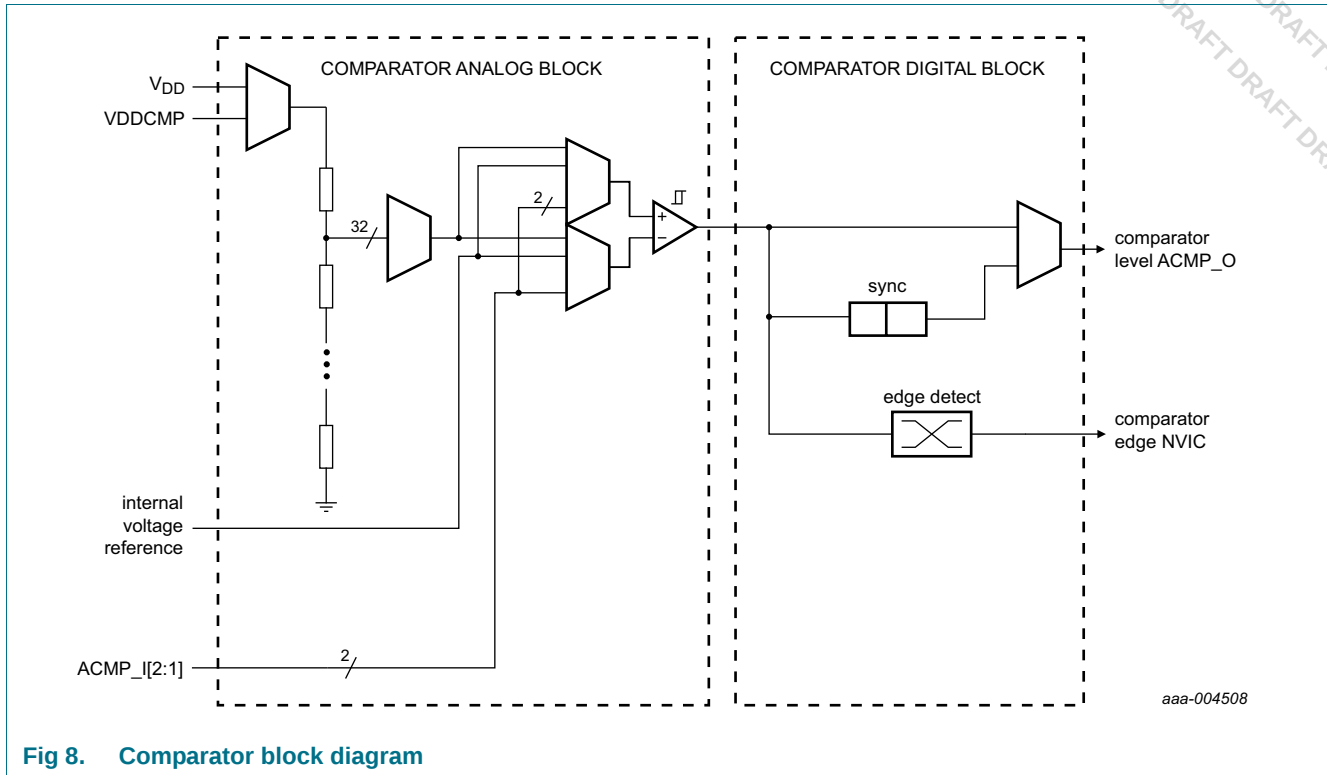


Fig 8. Comparator block diagram

7.19.1 Features

- Selectable 0 mV, 10 mV (± 5 mV), and 20 mV (± 10 mV), 40 mV (± 20 mV) input hysteresis.
- Two selectable external voltages (V_{DD} or VDDCMP on pin PIO0_6); fully configurable on either positive or negative input channel.
- Internal voltage reference from band gap and temperature sensor selectable on either positive or negative input channel.
- 32-stage voltage ladder with the internal reference voltage selectable on either the positive or the negative input channel.
- Voltage ladder source voltage is selectable from an external pin or the main 3.3 V supply voltage rail.
- Voltage ladder can be separately powered down for applications only requiring the comparator function.
- Interrupt output is connected to NVIC.
- Comparator level output is connected to output pin ACMP_O.
- The comparator output can be routed internally to the SCT input through the switch matrix.

7.20 Clocking and power control

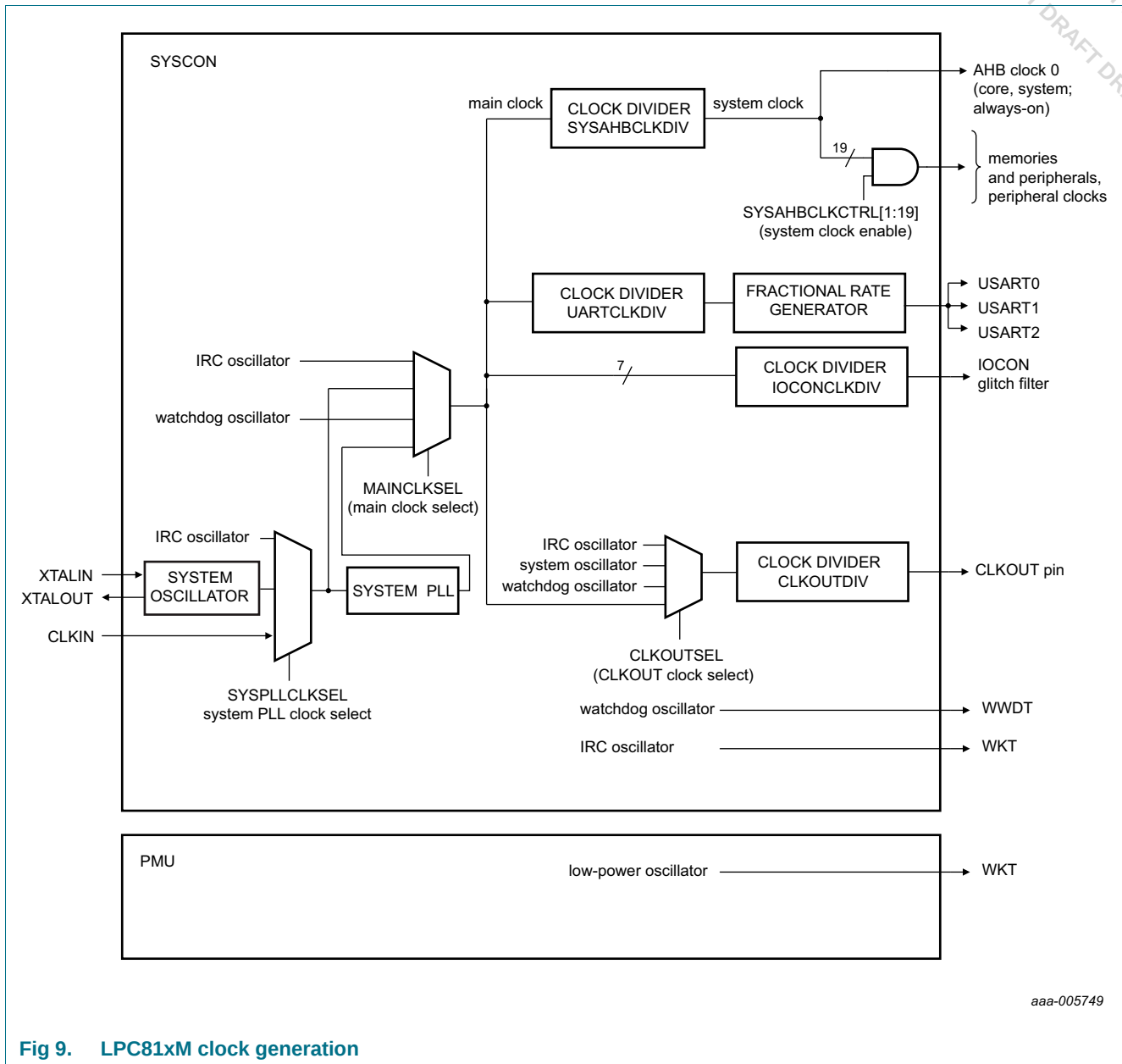


Fig 9. LPC81xM clock generation

7.20.1 Crystal and internal oscillators

The LPC81xM include four independent oscillators:

1. The crystal oscillator (SysOsc) operating at frequencies between 1 MHz and 25 MHz.
2. The internal RC Oscillator (IRC) with a fixed frequency of 12 MHz, trimmed to 1% accuracy.
3. The internal low-power, low-frequency Oscillator with a nominal frequency of 10 kHz with 40% accuracy for use with the self wake-up timer.
4. The dedicated Watchdog Oscillator (WDOsc) with a programmable nominal frequency between 9.4 kHz and 2.3 MHz with 40% accuracy.

Each oscillator, except the low-frequency oscillator, can be used for more than one purpose as required in a particular application.

Following reset, the LPC81xM will operate from the IRC until switched by software. This allows systems to operate without any external crystal and the bootloader code to operate at a known frequency.

See [Figure 9](#) for an overview of the LPC81xM clock generation.

7.20.1.1 Internal RC Oscillator (IRC)

The IRC may be used as the clock source for the WWDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 12 MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

The IRC can be used as a clock source for the CPU with or without using the PLL. The IRC frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

Upon power-up or any chip reset, the LPC81xM use the IRC as the clock source. Software may later switch to one of the other available clock sources.

7.20.1.2 Crystal Oscillator (SysOsc)

The crystal oscillator can be used as the clock source for the CPU, with or without using the PLL.

The SysOsc operates at frequencies of 1 MHz to 25 MHz. This frequency can be boosted to a higher frequency, up to the maximum CPU operating frequency, by the system PLL.

7.20.1.3 Internal Low-power Oscillator and Watchdog Oscillator (WDOsc)

The nominal frequency of the WDOsc is programmable between 9.4 kHz and 2.3 MHz. The frequency spread over silicon process variations is $\pm 40\%$.

The WDOsc is a dedicated oscillator for the windowed WWDT.

The internal low-power 10 kHz ($\pm 40\%$ accuracy) oscillator serves as the clock input to the WKT. This oscillator can be configured to run in all low power modes.

7.20.2 Clock input

A 3.3 V external clock source (25 MHz typical) can be supplied on the selected CLKIN pin or a 1.8 V external clock source can be supplied on the XTALIN pin (see [Section 13.1](#)).

7.20.3 System PLL

The PLL accepts an input clock frequency in the range of 10 MHz to 25 MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator (CCO). The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156 MHz to 320 MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source. The PLL settling time is nominally 100 μs .

7.20.4 Clock output

The LPC81xM features a clock output function that routes the IRC, the SysOsc, the watchdog oscillator, or the main clock to the CLKOUT function. The CLKOUT function can be connected to any digital pin through the switch matrix.

7.20.5 Wake-up process

The LPC81xM begin operation at power-up by using the IRC as the clock source. This allows chip operation to resume quickly. If the SysOsc, the external clock source, or the PLL is needed by the application, software must enable these features and wait for them to stabilize before they are used as a clock source.

7.20.6 Power control

The LPC81xM supports the ARM Cortex-M0 Sleep mode. The CPU clock rate may also be controlled as needed by changing clock sources, reconfiguring PLL values, and/or altering the CPU clock divider value. This allows a trade-off of power versus processing speed based on application requirements. In addition, a register is provided for shutting down the clocks to individual on-chip peripherals, allowing to fine-tune power consumption by eliminating all dynamic power use in any peripherals that are not required for the application. Selected peripherals have their own clock divider which provides even better power control.

7.20.6.1 Power profiles

The power consumption in Active and Sleep modes can be optimized for the application through simple calls to the power profile API. The API is accessible through the on-chip ROM.

The power configuration routine configures the LPC81xM for one of the following power modes:

- Default mode corresponding to power configuration after reset.
- CPU performance mode corresponding to optimized processing capability.
- Efficiency mode corresponding to optimized balance of current consumption and CPU performance.
- Low-current mode corresponding to lowest power consumption.

In addition, the power profile includes routines to select the optimal PLL settings for a given system clock and PLL input clock.

7.20.6.2 Sleep mode

When Sleep mode is entered, the clock to the core is stopped. Resumption from the Sleep mode does not need any special sequence but re-enabling the clock to the ARM core.

In Sleep mode, execution of instructions is suspended until either a reset or interrupt occurs. Peripheral functions continue operation during Sleep mode and may generate interrupts to cause the processor to resume execution. Sleep mode eliminates dynamic power used by the processor itself, memory systems and related controllers, and internal buses.

7.20.6.3 Deep-sleep mode

In Deep-sleep mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for the IRC and watchdog oscillator or low-power oscillator if selected. The IRC output is disabled. In addition all analog blocks are shut down and the flash is in stand-by mode. In Deep-sleep mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Deep-sleep mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Deep-sleep mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Deep-sleep mode saves power and allows for short wake-up times.

7.20.6.4 Power-down mode

In Power-down mode, the LPC81xM is in Sleep-mode and all peripheral clocks and all clock sources are off except for watchdog oscillator or low-power oscillator if selected. In addition all analog blocks and the flash are shut down. In Power-down mode, the application can keep the watchdog oscillator and the BOD circuit running for self-timed wake-up and BOD protection.

The LPC81xM can wake up from Power-down mode via a reset, digital pins selected as inputs to the pin interrupt block, a watchdog timer interrupt, or an interrupt from the USART (if the USART is configured in synchronous slave mode), the SPI, or the I2C blocks (in slave mode).

Any interrupt used for waking up from Power-down mode must be enabled in one of the SYSCON wake-up enable registers and the NVIC.

Power-down mode reduces power consumption compared to Deep-sleep mode at the expense of longer wake-up times.

7.20.6.5 Deep power-down mode

In Deep power-down mode, power is shut off to the entire chip except for the WAKEUP pin and the self wake-up timer if enabled. The LPC81xM can wake up from Deep power-down mode via the WAKEUP pin, or without an external signal by using the time-out of the self wake-up timer (see [Section 7.18](#)).

The LPC81xM can be prevented from entering Deep power-down mode by setting a lock bit in the PMU block. Locking out Deep power-down mode enables the application to keep the watchdog timer or the BOD running at all times.

When entering Deep power-down mode, an external pull-up resistor is required on the WAKEUP pin to hold it HIGH. Pull the RESET pin HIGH to prevent it from floating while in Deep power-down mode.

7.21 System control

7.21.1 Reset

Reset has four sources on the LPC81xM: the $\overline{\text{RESET}}$ pin, the Watchdog reset, power-on reset (POR), and the BrownOut Detection (BOD) circuit. The $\overline{\text{RESET}}$ pin is a Schmitt trigger input pin. Assertion of chip reset by any source, once the operating voltage attains a usable level, starts the IRC and initializes the flash controller.

A LOW-going pulse as short as 50 ns resets the part.

When the internal Reset is removed, the processor begins executing at address 0, which is initially the Reset vector mapped from the boot block. At that point, all of the processor and peripheral registers have been initialized to predetermined values.

In Deep power-down mode, an external pull-up resistor is required on the $\overline{\text{RESET}}$ pin.

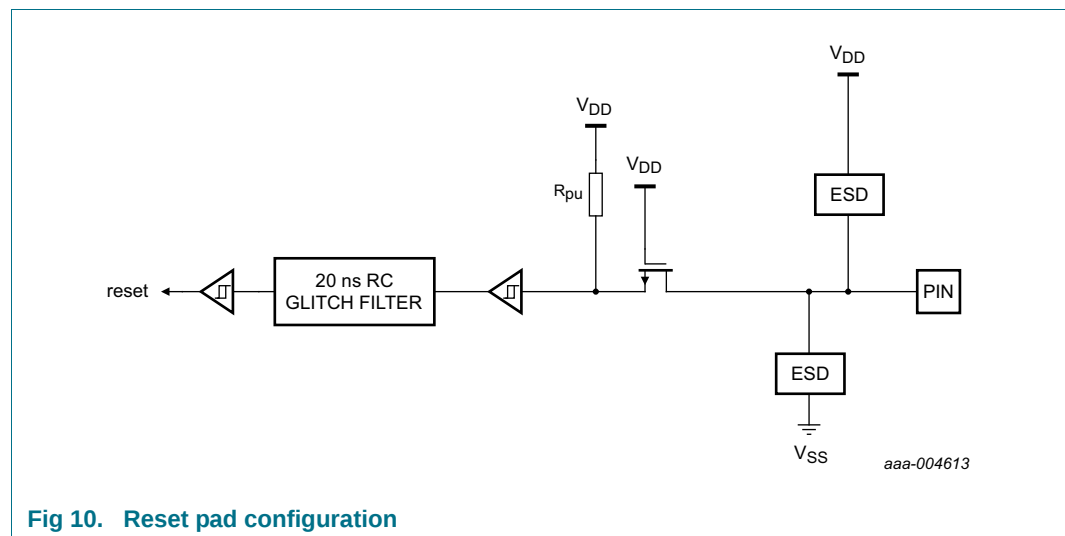


Fig 10. Reset pad configuration

7.21.2 Brownout detection

The LPC81xM includes up to four levels for monitoring the voltage on the V_{DD} pin. If this voltage falls below one of the selected levels, the BOD asserts an interrupt signal to the NVIC. This signal can be enabled for interrupt in the Interrupt Enable Register in the NVIC to cause a CPU interrupt. Alternatively, software can monitor the signal by reading a dedicated status register. Four threshold levels can be selected to cause a forced reset of the chip.

7.21.3 Code security (Code Read Protection - CRP)

CRP provides different levels of security in the system so that access to the on-chip flash and use of the Serial Wire Debugger (SWD) and In-System Programming (ISP) can be restricted. Programming a specific pattern into a dedicated flash location invokes CRP. IAP commands are not affected by the CRP.

In addition, ISP entry via the PIO0_1 pin can be disabled without enabling CRP. For details, see the *LPC800 user manual*.

There are three levels of Code Read Protection:

1. CRP1 disables access to the chip via the SWD and allows partial flash update (excluding flash sector 0) using a limited set of the ISP commands. This mode is useful when CRP is required and flash field updates are needed but all sectors cannot be erased.
2. CRP2 disables access to the chip via the SWD and only allows full flash erase and update using a reduced set of the ISP commands.
3. Running an application with level CRP3 selected, fully disables any access to the chip via the SWD pins and the ISP. This mode effectively disables ISP override using PIO0_1 pin as well. If necessary, the application must provide a flash update mechanism using IAP calls or using a call to the reinvoke ISP command to enable flash update via the USART.

CAUTION

If level three Code Read Protection (CRP3) is selected, no future factory testing can be performed on the device.

In addition to the three CRP levels, sampling of pin PIO0_1 for valid user code can be disabled. For details, see the *LPC800 user manual*.

7.21.4 APB interface

The APB peripherals are located on one APB bus.

7.21.5 AHBLite

The AHBLite connects the CPU bus of the ARM Cortex-M0+ to the flash memory, the main static RAM, the CRC, and the ROM.

7.22 Emulation and debugging

Debug functions are integrated into the ARM Cortex-M0+. Serial wire debug functions are supported in addition to a standard JTAG boundary scan. The ARM Cortex-M0+ is configured to support up to four breakpoints and two watch points.

The Micro Trace Buffer is implemented on the LPC81xM.

The $\overline{\text{RESET}}$ pin selects between the JTAG boundary scan ($\overline{\text{RESET}} = \text{LOW}$) and the ARM SWD debug ($\overline{\text{RESET}} = \text{HIGH}$). The ARM SWD debug port is disabled while the LPC81xM is in reset. The JTAG boundary scan pins are selected by hardware when the part is in boundary scan mode on pins PIO0_0 to PIO0_3 (see [Table 3](#)).

To perform boundary scan testing, follow these steps:

1. Erase any user code residing in flash.
2. Power up the part with the $\overline{\text{RESET}}$ pin pulled HIGH externally.
3. Wait for at least 250 μs .
4. Pull the $\overline{\text{RESET}}$ pin LOW externally.
5. Perform boundary scan operations.
6. Once the boundary scan operations are completed, assert the $\overline{\text{TRST}}$ pin to enable the SWD debug mode, and release the $\overline{\text{RESET}}$ pin (pull HIGH).

Remark: The JTAG interface cannot be used for debug purposes.

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage (core and external rail)		^[2] -0.5	+4.6	V
V _I	input voltage	5 V tolerant I/O pins; only valid when the V _{DD} supply voltage is present	^[3] -0.5	+5.5	V
		5 V open-drain pins PIO0_10 and PIO0_11	^[4] -0.5	+5.5	V
		3 V tolerant I/O pin PIO0_6	^[5] -0.5	+3.6	V
V _{IA}	analog input voltage		^[6] -0.5 V ^[7]	4.6	V
V _{i(xtal)}	crystal input voltage		^[2] -0.5	+2.5	V
I _{DD}	supply current	per supply pin	-	100	mA
I _{SS}	ground current	per ground pin	-	100	mA
I _{latch}	I/O latch-up current	-(0.5V _{DD}) < V _I < (1.5V _{DD}); T _J < 125 °C	-	100	mA
T _{stg}	storage temperature	non-operating	^[8] -65	+150	°C
T _{J(max)}	maximum junction temperature		-	150	°C
P _{tot(pack)}	total power dissipation (per package)	based on package heat transfer, not device power consumption	-	<tbid>	W
V _{ESD}	electrostatic discharge voltage	human body model; all pins	^[9] -	<tbid>	V

- [1] The following applies to the limiting values:
- a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
 - b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.
 - c) The limiting values are stress ratings only and operating the part at these values is not recommended and proper operation is not guaranteed. The conditions for functional operation are specified in [Table 9](#).
- [2] Maximum/minimum voltage above the maximum operating voltage (see [Table 9](#)) and below ground that can be applied for a short time (< 10 ms) to a device without leading to irrecoverable failure. Failure includes the loss of reliability and shorter lifetime of the device.
- [3] Including voltage on outputs in tri-state mode. Does not apply to pin PIO0_6.
- [4] V_{DD} present or not present. Compliant with the I²C-bus standard. 5.5 V can be applied to this pin when V_{DD} is powered down.
- [5] V_{DD} present or not present.
- [6] If the comparator is configured with the common mode input V_{IC} = V_{DD}, the other comparator input can be up to 0.2 V above or below V_{DD} without affecting the hysteresis range of the comparator function.
- [7] It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

- [8] The maximum non-operating storage temperature is different than the temperature for required shelf life which should be determined based on required shelf lifetime. Please refer to the JEDEC spec (J-STD-033B.1) for further details.
- [9] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 k Ω series resistor.

9. Thermal characteristics

The average chip junction temperature, T_j ($^{\circ}\text{C}$), can be calculated using the following equation:

$$T_j = T_{amb} + (P_D \times R_{th(j-a)}) \quad (1)$$

- T_{amb} = ambient temperature ($^{\circ}\text{C}$),
- $R_{th(j-a)}$ = the package junction-to-ambient thermal resistance ($^{\circ}\text{C/W}$)
- P_D = sum of internal and I/O power dissipation

The internal power dissipation is the product of I_{DD} and V_{DD} . The I/O power dissipation of the I/O pins is often small and many times can be negligible. However it can be significant in some applications.

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{j(max)}$	maximum junction temperature		-	-	125	$^{\circ}\text{C}$

Table 7. Thermal resistance (TSSOP packages)

Symbol	Parameter	Conditions	Thermal resistance in $^{\circ}\text{C/W}$ $\pm 15\%$	
			TSSOP16	TSSOP20
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in $\times$ 4 in); still air	<td>	<td>
		Single-layer (4.5 in $\times$ 3 in); still air	<td>	<td>
$R_{th(j-c)}$	thermal resistance from junction to case		<td>	<td>

Table 8. Thermal resistance value (SO/DIP packages)

Symbol	Parameter	Conditions	Thermal resistance in $^{\circ}\text{C/W}$ $\pm 15\%$	
			SO20	DIP8
$R_{th(j-a)}$	thermal resistance from junction to ambient	JEDEC (4.5 in $\times$ 4 in); still air	<td>	<td>
		8-layer (4.5 in $\times$ 3 in); still air	<td>	<td>
$R_{th(j-c)}$	thermal resistance from junction to case		<td>	<td>

10. Static characteristics

Table 9. Static characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
V_{DD}	supply voltage (core and external rail)		1.8	3.3	3.6	V
I_{DD}	supply current	Active mode; code while(1){} executed from flash				
		system clock = 12 MHz; default mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	1.4	- mA
		system clock = 12 MHz; low-current mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	<tb>	- mA
		system clock = 30 MHz; default mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [6] [7] [8]	-	5.5	- mA
		system clock = 30 MHz; low-current mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [6] [7] [8]	-	<tb>	- mA
		Sleep mode; system clock = 12 MHz; default mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	0.8	- mA
		system clock = 12 MHz; low-current mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	<tb>	- mA
		system clock = 30 MHz; default mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	2.6	- mA
		system clock = 30 MHz; low-current mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [4] [6] [7]	-	<tb>	- mA
		Deep-sleep mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [9]	-	170	- μA
		Power-down mode; $V_{DD} = 3.3\text{ V}$	[2] [3] [9]	-	2	- μA
		Deep power-down mode; $V_{DD} = 3.3\text{ V}$	[2] [10]	-	220	- nA
		Low-power oscillator off				
		Low-power oscillator on/WKT wake-up enabled			<tb>	- nA
Standard port pins configured as digital pins, RESET, see Figure 11						
I_{IL}	LOW-level input current	$V_I = 0\text{ V}$; on-chip pull-up resistor disabled	-	<tb>	<tb>	nA
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; on-chip pull-down resistor disabled	-	<tb>	<tb>	nA
I_{OZ}	OFF-state output current	$V_O = 0\text{ V}$; $V_O = V_{DD}$; on-chip pull-up/down resistors disabled	-	<tb>	<tb>	nA
V_I	input voltage	$V_{DD} \geq 1.8\text{ V}$; 5 V tolerant pins except PIO0_6	[12] [14]	0	-	5 V
		$V_{DD} \geq 1.8\text{ V}$; on 3 V tolerant pin PIO0_6		0	-	3.6
		$V_{DD} = 0\text{ V}$		0	-	3.6 V

Table 9. Static characteristics ...continued

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _O	output voltage	output active	0	-	<tbid>	V
V _{IH}	HIGH-level input voltage		<tbid>	-	-	V
V _{IL}	LOW-level input voltage		-	-	<tbid>	V
V _{hys}	hysteresis voltage		<tbid>	-	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −4 mA	<tbid>	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −3 mA	<tbid>	-	-	V
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	<tbid>	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	<tbid>	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	mA
I _{OHS}	HIGH-level short-circuit output current	V _{OH} = 0 V	^[15] -	-	<tbid>	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD}	^[15] -	-	<tbid>	mA
I _{pd}	pull-down current	V _I = 5 V	<tbid>	<tbid>	<tbid>	μA
I _{pu}	pull-up current	V _I = 0 V; 2.0 V ≤ V _{DD} ≤ 3.6 V	<tbid>	<tbid>	<tbid>	μA
		1.8 V ≤ V _{DD} < 2.0 V	<tbid>	<tbid>	<tbid>	μA
		V _{DD} < V _I < 5 V	<tbid>	<tbid>	<tbid>	μA
High-drive output pins configured as digital pins (PIO0_2, PIO0_3, PIO0_7, PIO0_12, PIO0_13) see Figure 11						
I _{IL}	LOW-level input current	V _I = 0 V; on-chip pull-up resistor disabled	-	<tbid>	<tbid>	nA
I _{IH}	HIGH-level input current	V _I = V _{DD} ; on-chip pull-down resistor disabled	-	<tbid>	<tbid>	nA
I _{OZ}	OFF-state output current	V _O = 0 V; V _O = V _{DD} ; on-chip pull-up/down resistors disabled	-	<tbid>	<tbid>	nA
V _I	input voltage	V _{DD} ≥ 1.8 V	^[12] 0 ^[14]	-	5	V
		V _{DD} = 0 V	0	-	3.6	V
V _O	output voltage	output active	<tbid>	-	<tbid>	V
V _{IH}	HIGH-level input voltage		<tbid>	-	-	V
V _{IL}	LOW-level input voltage		-	-	<tbid>	V
V _{hys}	hysteresis voltage		<tbid>	-	-	V
V _{OH}	HIGH-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OH} = −20 mA	<tbid>	-	-	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OH} = −12 mA	<tbid>	-	-	V

Table 9. Static characteristics ...continued $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{OL}	LOW-level output voltage	2.5 V ≤ V _{DD} ≤ 3.6 V; I _{OL} = 4 mA	-	-	<tbid>	V
		1.8 V ≤ V _{DD} < 2.5 V; I _{OL} = 3 mA	-	-	<tbid>	V
I _{OH}	HIGH-level output current	V _{OH} = V _{DD} − 0.4 V; 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	mA
I _{OL}	LOW-level output current	V _{OL} = 0.4 V 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	mA
I _{OLS}	LOW-level short-circuit output current	V _{OL} = V _{DD}	^[15] -	-	<tbid>	mA
I _{pd}	pull-down current	V _I = 5 V	<tbid>	<tbid>	<tbid>	μA
I _{pu}	pull-up current	V _I = 0 V 2.0 V ≤ V _{DD} ≤ 3.6 V	<tbid>	<tbid>	<tbid>	μA
		1.8 V ≤ V _{DD} < 2.0 V	<tbid>	<tbid>	<tbid>	μA
		V _{DD} < V _I < 5 V	<tbid>	<tbid>	<tbid>	μA
I ² C-bus pins (PIO0_10 and PIO0_11) see Figure 11						
V _{IH}	HIGH-level input voltage		<tbid>	-	-	V
V _{IL}	LOW-level input voltage		-	-	<tbid>	V
V _{hys}	hysteresis voltage		-	<tbid>	-	V
I _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as standard mode pins 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	
I _{OL}	LOW-level output current	V _{OL} = 0.4 V; I ² C-bus pins configured as Fast-mode Plus pins 2.5 V ≤ V _{DD} ≤ 3.6 V	<tbid>	-	-	mA
		1.8 V ≤ V _{DD} < 2.5 V	<tbid>	-	-	
I _{LI}	input leakage current	V _I = V _{DD}	^[16] -	<tbid>	<tbid>	μA
		V _I = 5 V	-	<tbid>	<tbid>	μA
Oscillator input pins (PIO0_8 and PIO0_9)						
V _{i(xtal)}	crystal input voltage		<tbid>	<tbid>	<tbid>	V
V _{o(xtal)}	crystal output voltage		<tbid>	<tbid>	<tbid>	V

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] $T_{amb} = 25\text{ }^{\circ}\text{C}$.

[3] I_{DD} measurements were performed with all pins configured as GPIO outputs driven LOW and pull-up resistors disabled.

[4] IRC enabled; system oscillator disabled; system PLL disabled.

[5] System oscillator enabled; IRC disabled; system PLL disabled.

[6] BOD disabled.

[7] All peripherals disabled in the SYSAHBCLKCTRL register. Peripheral clocks to USART, CLKOUT, and IOCON disabled in system configuration block.

[8] IRC disabled; system oscillator enabled; system PLL enabled.

- [9] All oscillators and analog blocks turned off in the PDSLEEPCFG register; PDSLEEPCFG = 0x0000 18FF.
- [10] WAKEUP pin pulled HIGH externally.
- [11] Low-current mode PWR_LOW_CURRENT selected when running the set_power routine in the power profiles.
- [12] Including voltage on outputs in 3-state mode.
- [13] V_{DD} supply voltage must be present.
- [14] 3-state outputs go into 3-state mode in Deep power-down mode.
- [15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.
- [16] To V_{SS} .

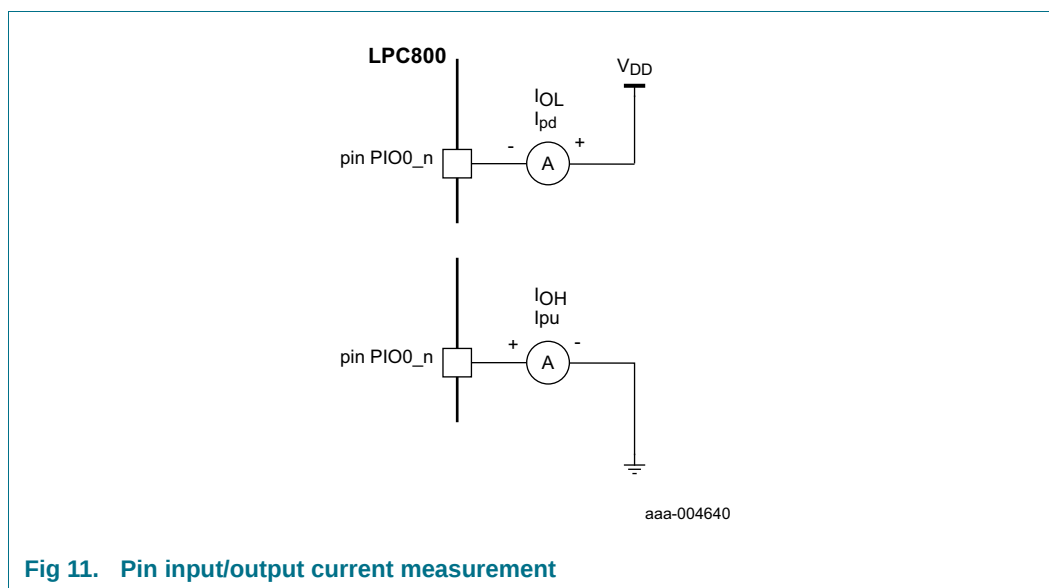
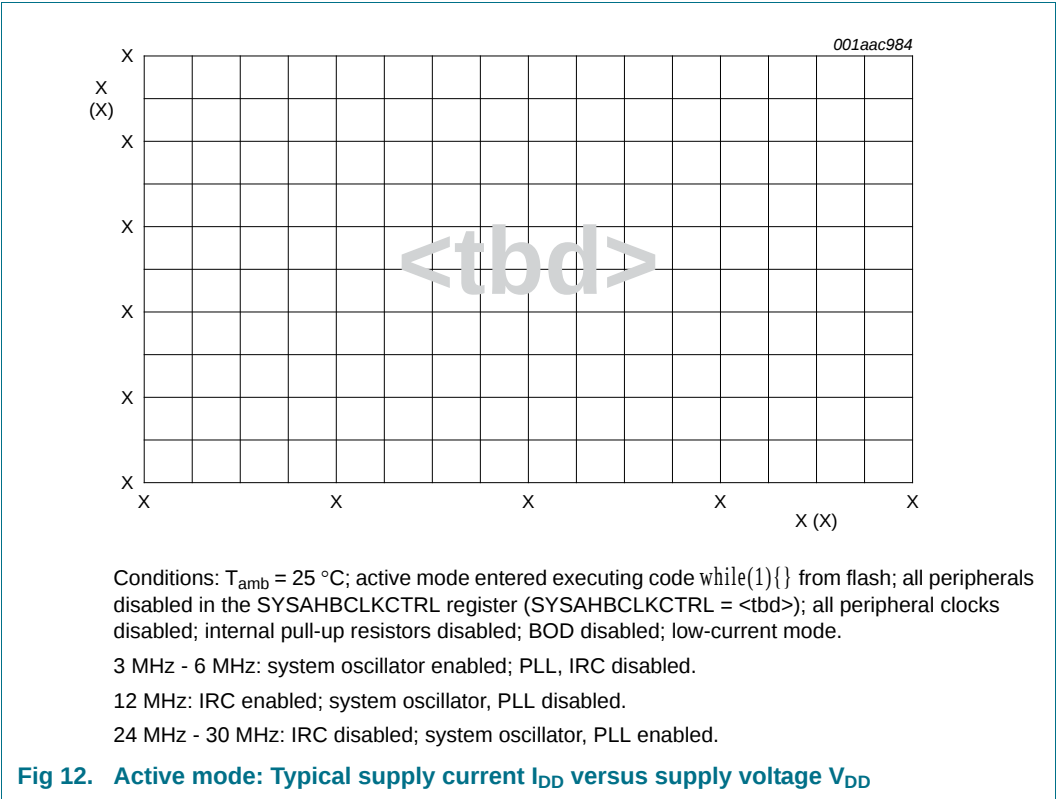


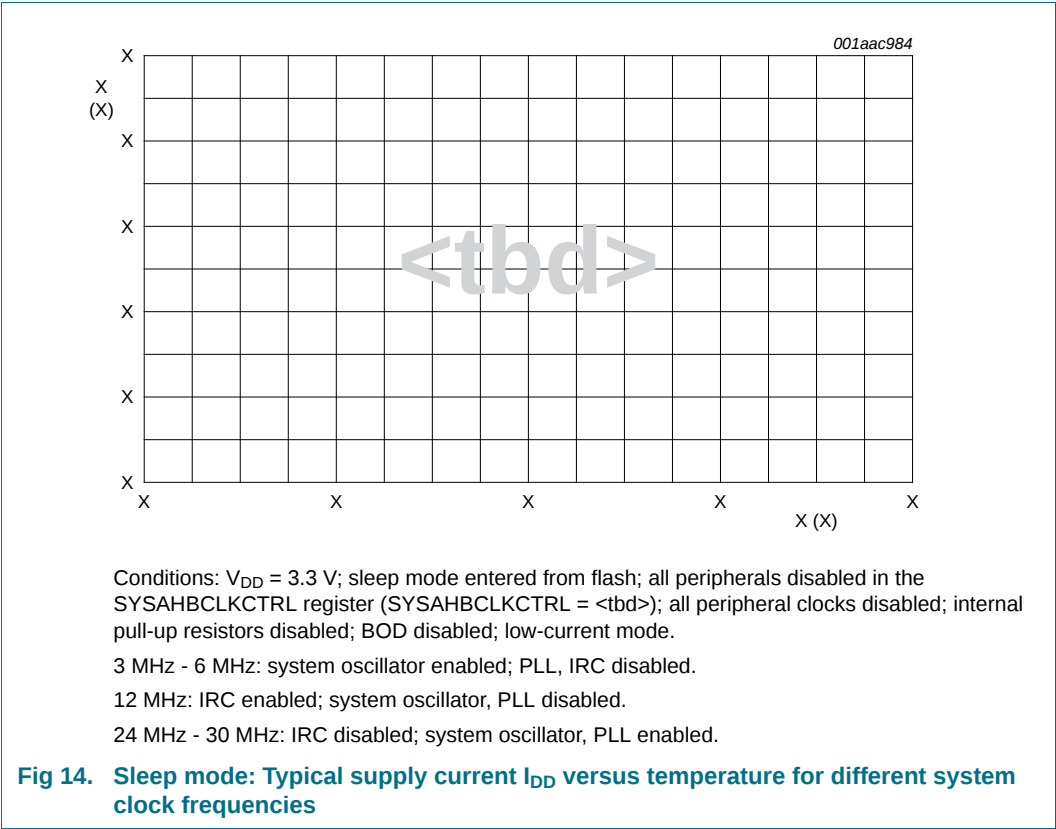
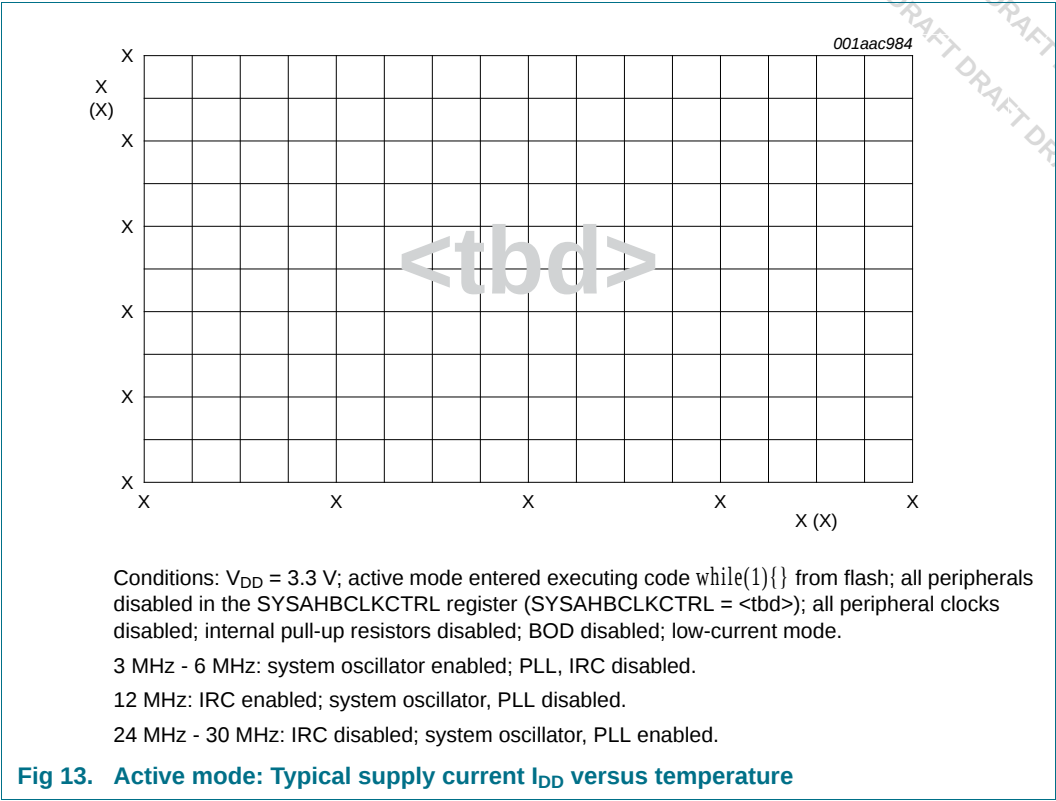
Fig 11. Pin input/output current measurement

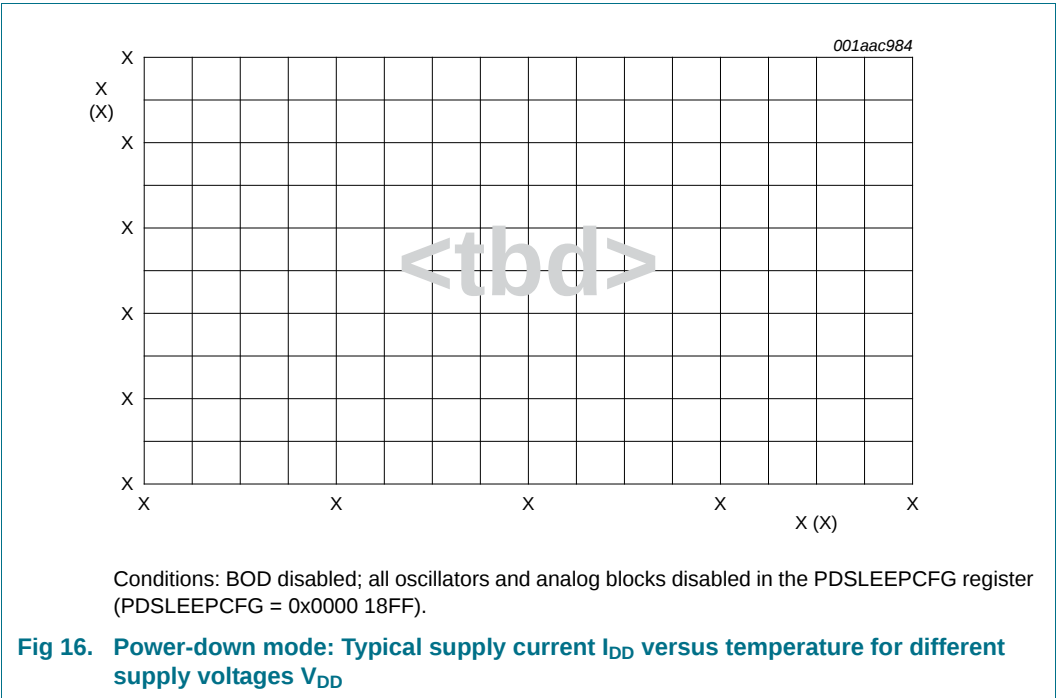
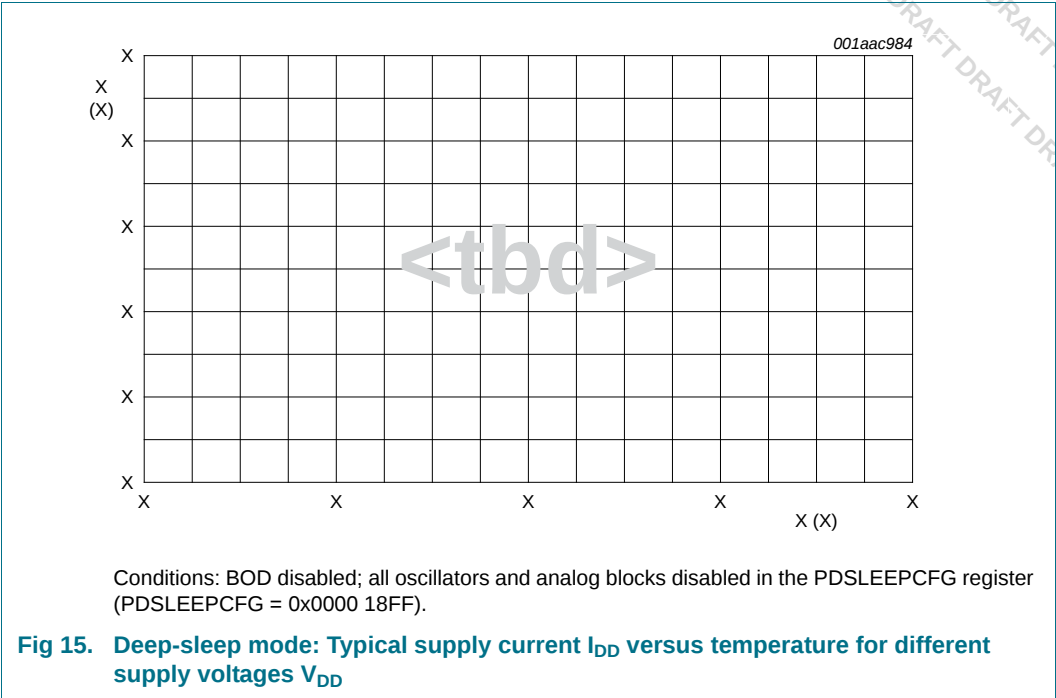
10.1 Power consumption

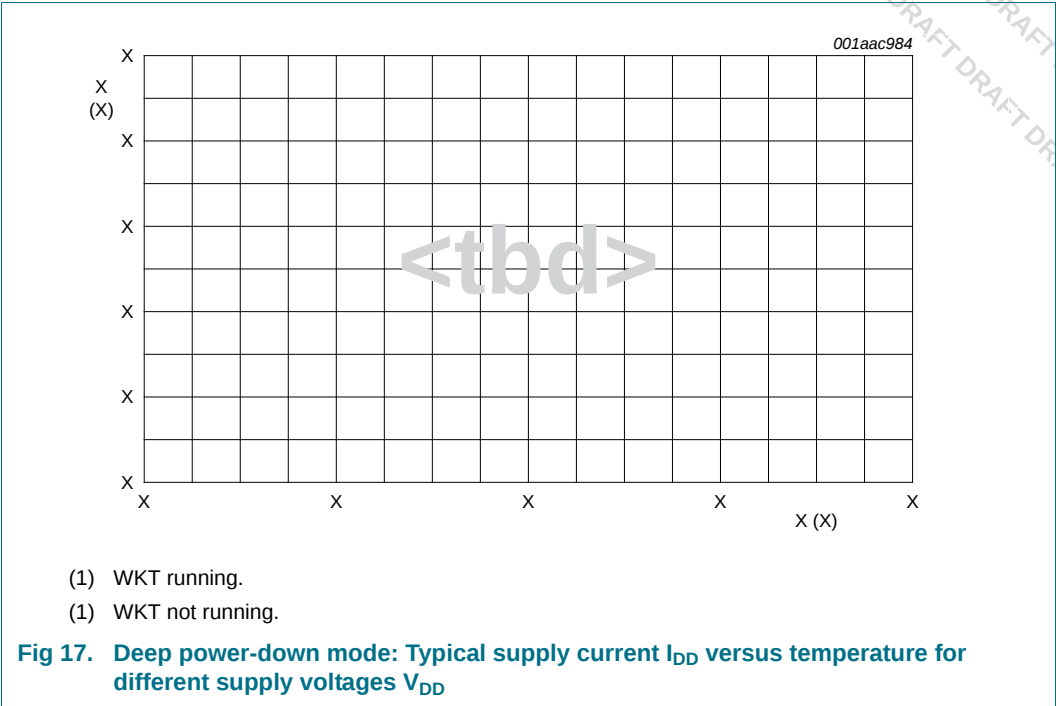
Power measurements in Active, Sleep, and Deep-sleep modes were performed under the following conditions):

- Configure all pins as GPIO with pull-up resistor disabled in the IOCON block.
- Configure GPIO pins as outputs using the GPIO DIR register.
- Write 0 to all GPIO DATA register to drive the outputs LOW.

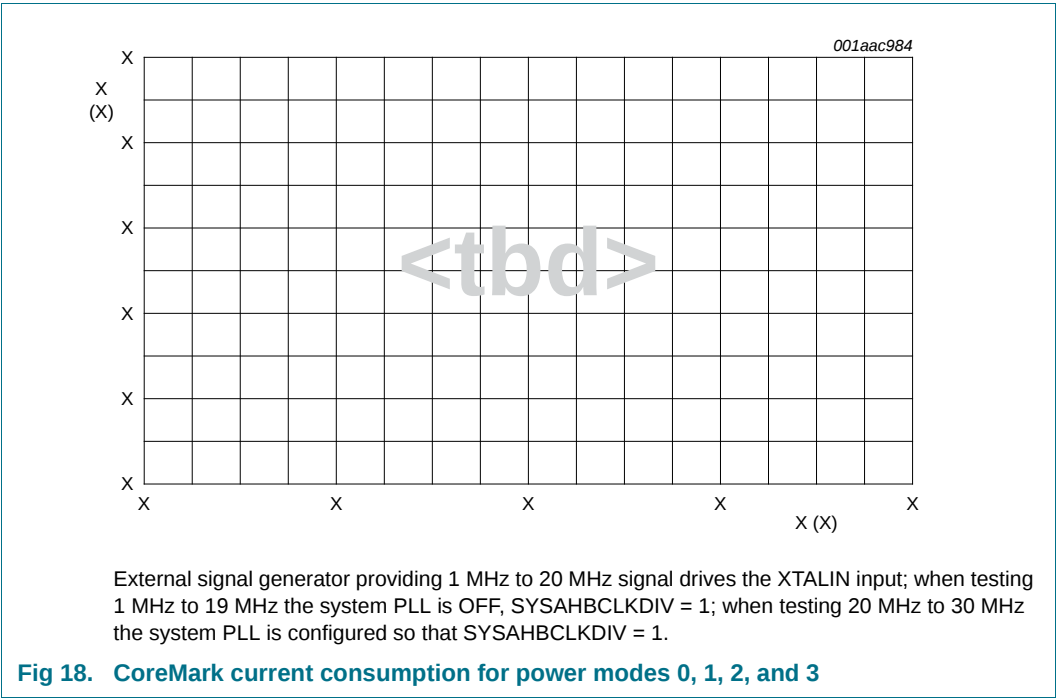








10.2 CoreMark data



10.3 Peripheral power consumption

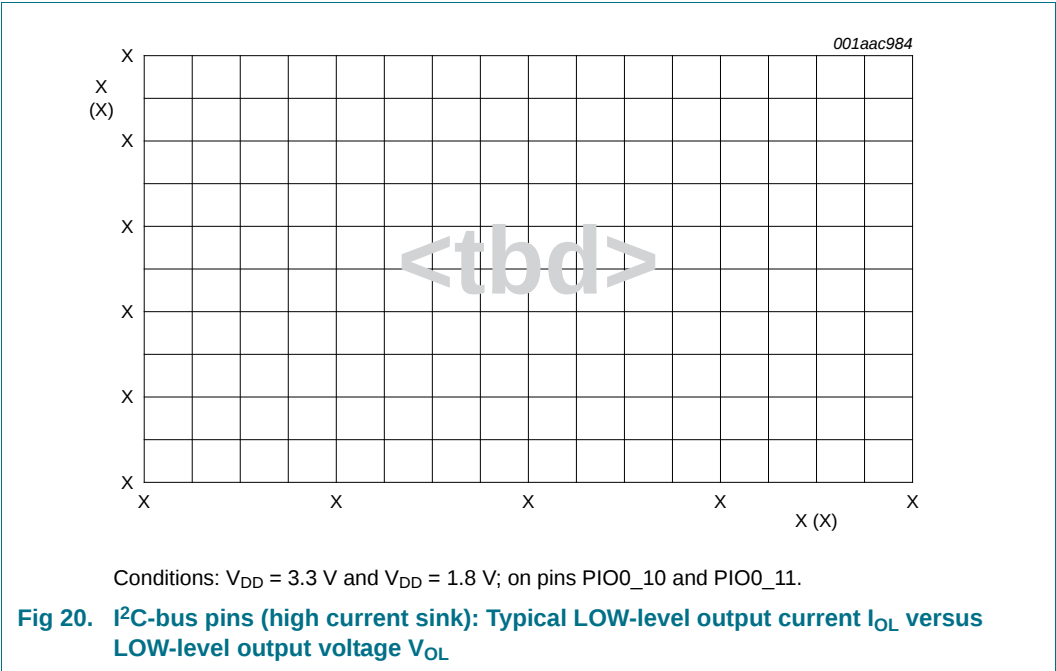
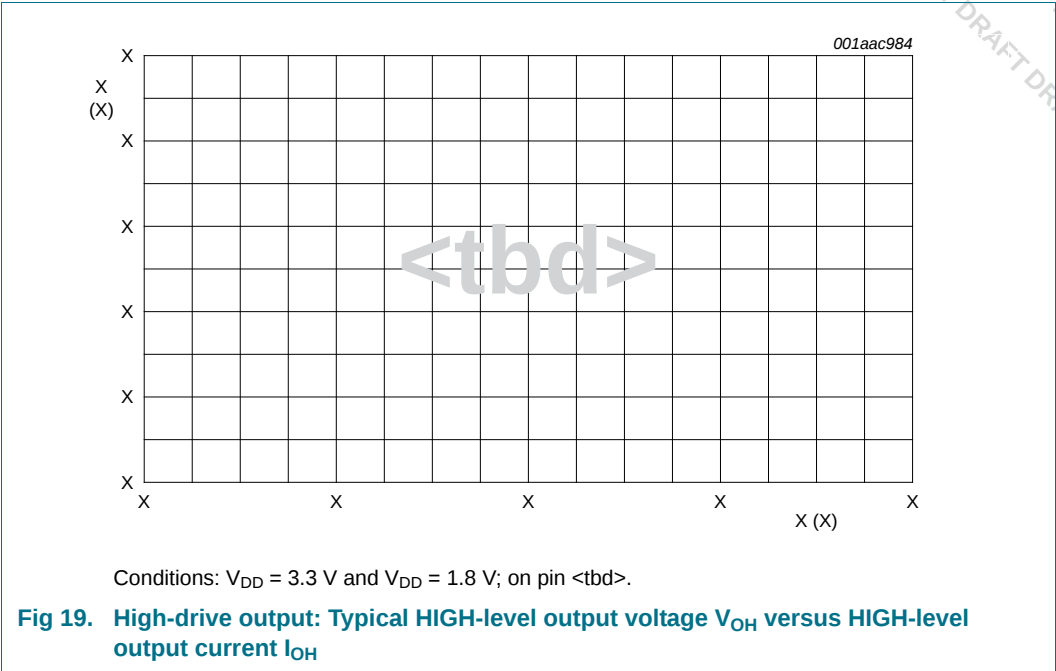
The supply current per peripheral is measured as the difference in supply current between the peripheral block enabled and the peripheral block disabled in the SYSAHBCLKCFG and PDRUNCFG (for analog blocks) registers. All other blocks are disabled in both registers and no code is executed. Measured on a typical sample at $T_{amb} = 25\text{ }^{\circ}\text{C}$. Unless noted otherwise, the system oscillator and PLL are running in both measurements.

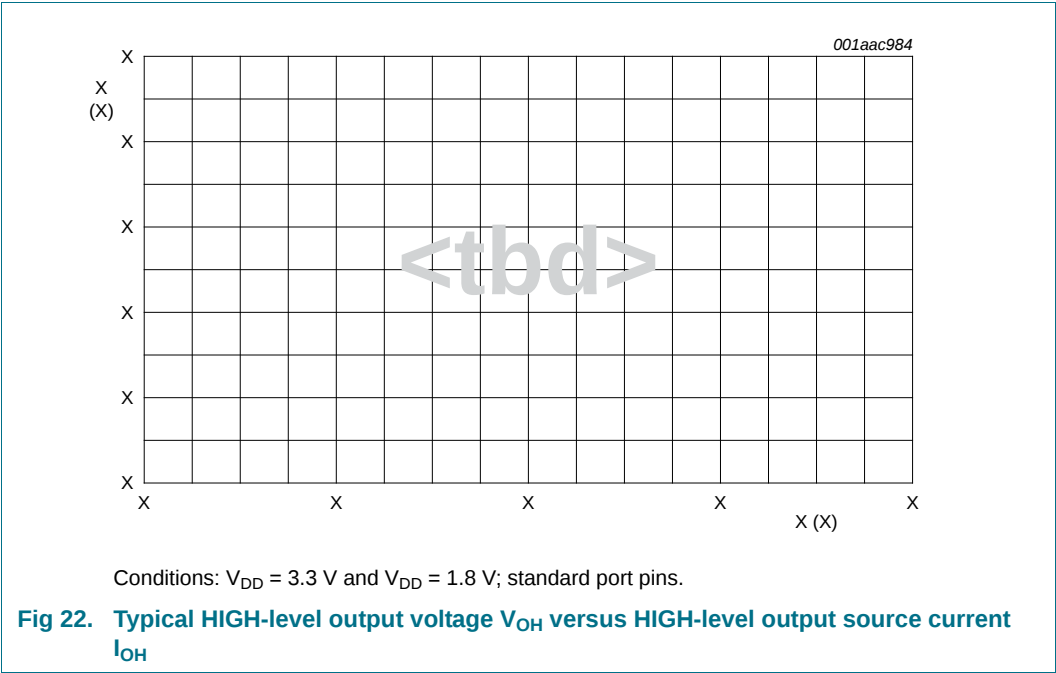
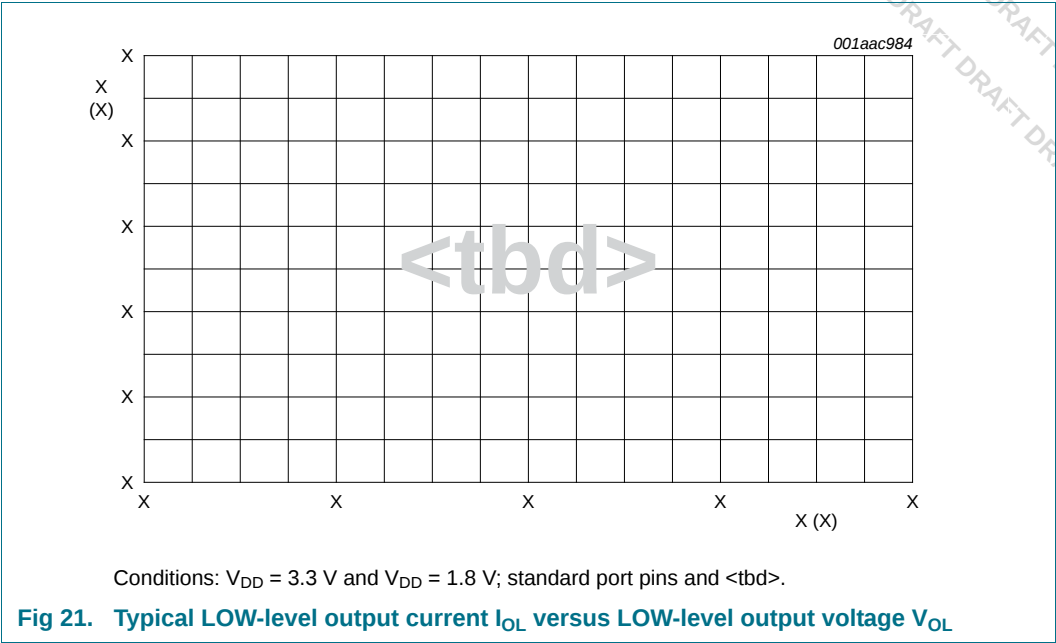
The supply currents are shown for system clock frequencies of 12 MHz and 30 MHz.

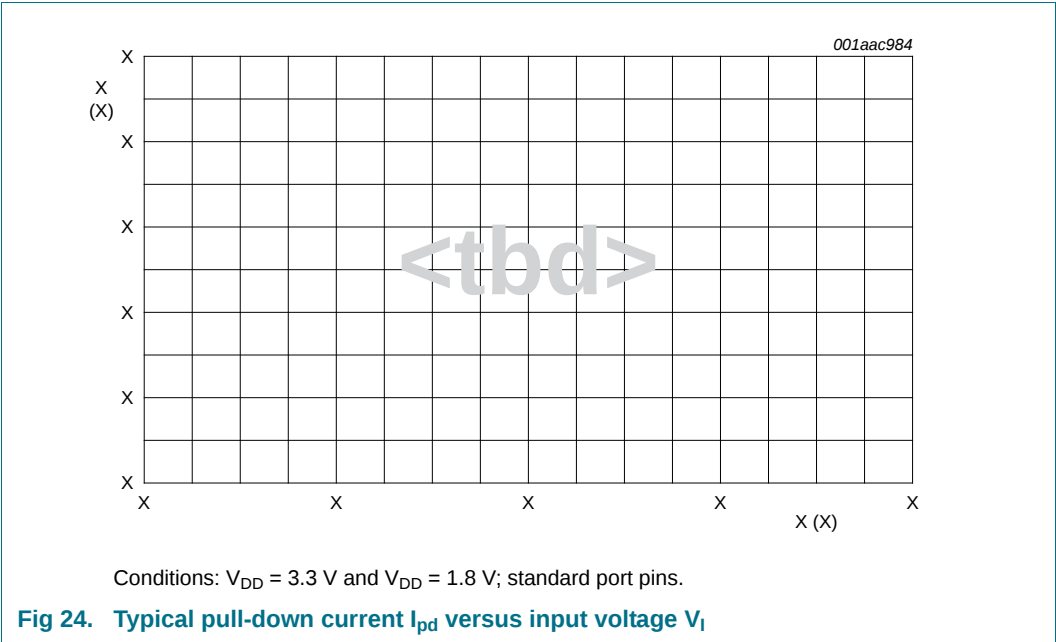
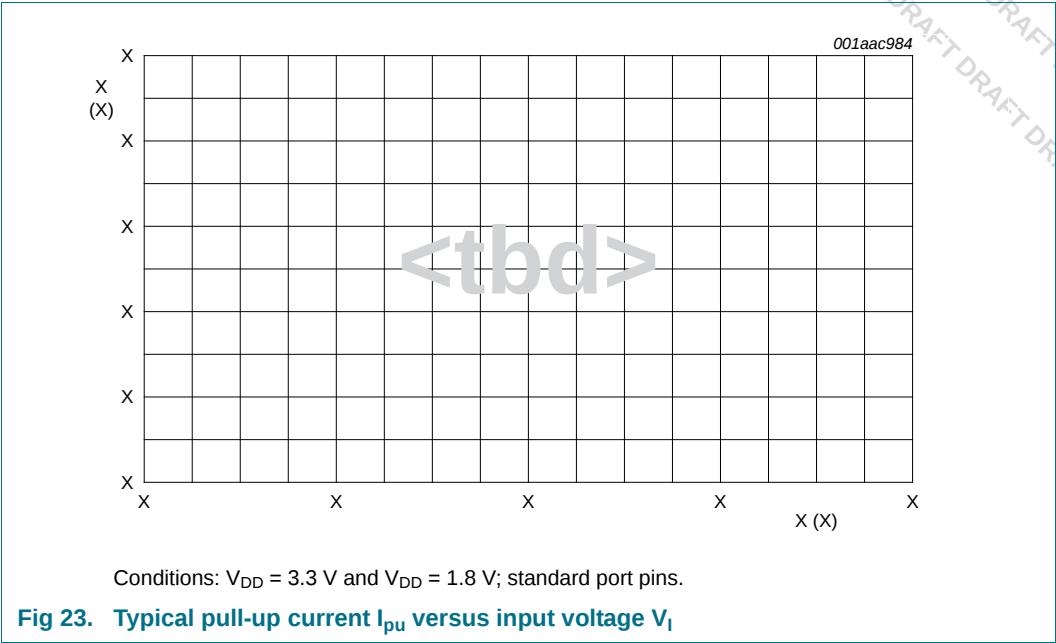
Table 10. Power consumption for individual analog and digital blocks

Peripheral	Typical supply current in mA			Notes
	n/a	12 MHz	30 MHz	
IRC	<td>	-	-	System oscillator running; PLL off; independent of main clock frequency.
System oscillator at 12 MHz	<td>	-	-	IRC running; PLL off; independent of main clock frequency.
Watchdog oscillator at 500 kHz/2	<td>	-	-	System oscillator running; PLL off; independent of main clock frequency.
BOD	<td>	-	-	Independent of main clock frequency.
Main PLL	-	<td>	-	-
CLKOUT	-	<td>	<td>	Main clock divided by 4 in the CLKOUTDIV register.
SCT	-	<td>	<td>	-
MRT	-	<td>	<td>	-
WKT	-	<td>	<td>	-
GPIO	-	<td>	<td>	GPIO pins configured as outputs and set to LOW. Direction and pin state are maintained if the GPIO is disabled in the SYSAHBCLKCFG register.
Pin interrupt/pattern match		<td>	<td>	-
IOCON	-	<td>	<td>	-
I2C	-	<td>	<td>	-
ROM	-	<td>	<td>	-
SPI0	-	<td>	<td>	-
SPI1	-	<td>	<td>	-
USART0	-	<td>	<td>	-
USART1	-	<td>	<td>	-
USART2	-	<td>	<td>	-
WWDT	-	<td>	<td>	Main clock selected as clock source for the WDT.
Comparator	-	<td>	<td>	-
CRC	-	<td>	<td>	-
SWM	-	<td>	<td>	-

10.4 Electrical pin characteristics







11. Dynamic characteristics

11.1 Power-up ramp conditions

<tbid>

11.2 Flash memory

Table 11. Flash characteristics

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$. Based on JEDEC NVM qualification. Failure rate < 10 ppm for parts as specified below.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{endu}	endurance		[2][1] 10 000	100 000	-	cycles
t_{ret}	retention time	powered	[2] 10	20	-	years
		unpowered	[2] 20	40	-	years
t_{er}	erase time	sector or multiple consecutive sectors	[2] 95	100	105	ms
t_{prog}	programming time		[2][3] 0.95	1	1.05	ms

[1] Number of program/erase cycles.

[2] Min and max values are valid for $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ only.

[3] Programming times are given for writing <tbid> bytes to the flash. $T_{amb} < +85\text{ }^{\circ}\text{C}$. Data must be written to the flash in blocks of 256 bytes. Flash programming is accomplished via IAP calls (see *LPC800 user manual*). Execution time of IAP calls depends on the system clock and is typically between 1.5 and 2 ms per 256 bytes.

11.3 External clock for the oscillator in slave mode and CLKIN

Remark: The input voltage on the XTAL1/2 pins must be $\leq 1.95\text{ V}$ (see [Table 9](#)). For connecting the oscillator to the XTAL pins, also see [Section 13.1](#).

Table 12. Dynamic characteristic: external clock (XTALIN or CLKIN inputs)

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; V_{DD} over specified ranges. [1]

Symbol	Parameter	Conditions	Min	Typ [2]	Max	Unit
f_{osc}	oscillator frequency		1	-	25	MHz
$T_{cy(clk)}$	clock cycle time		40	-	1000	ns
t_{CHCX}	clock HIGH time	$T_{cy(clk)} \times 0.4$	-	-	-	ns
t_{CLCX}	clock LOW time	$T_{cy(clk)} \times 0.4$	-	-	-	ns
t_{CLCH}	clock rise time		-	-	5	ns
t_{CHCL}	clock fall time		-	-	5	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature ($25\text{ }^{\circ}\text{C}$), nominal supply voltages.

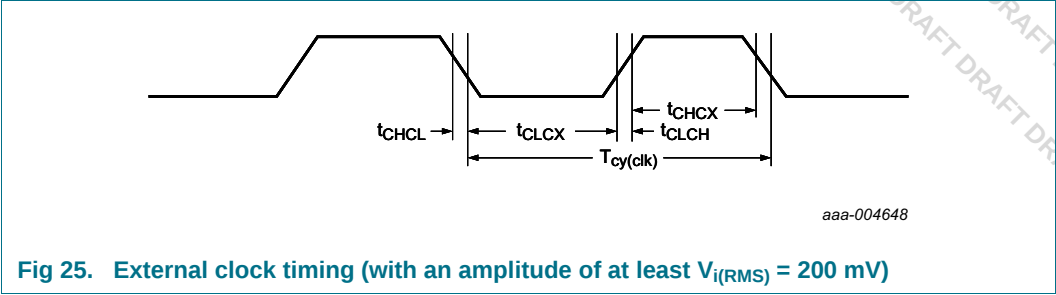


Fig 25. External clock timing (with an amplitude of at least $V_{i(RMS)} = 200\text{ mV}$)

11.4 Internal oscillators

Table 13. Dynamic characteristic: internal oscillators

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; $2.7\text{ V} \leq V_{DD} \leq 3.6\text{ V}$.^[1]

Symbol	Parameter	Conditions	Min	Typ ^[2]	Max	Unit
$f_{osc(RC)}$	internal RC oscillator frequency	-	11.88	12	12.12	MHz

- [1] Parameters are valid over operating temperature range unless otherwise specified.
- [2] Typical ratings are not guaranteed. The values listed are at room temperature ($25\text{ }^{\circ}\text{C}$), nominal supply voltages.

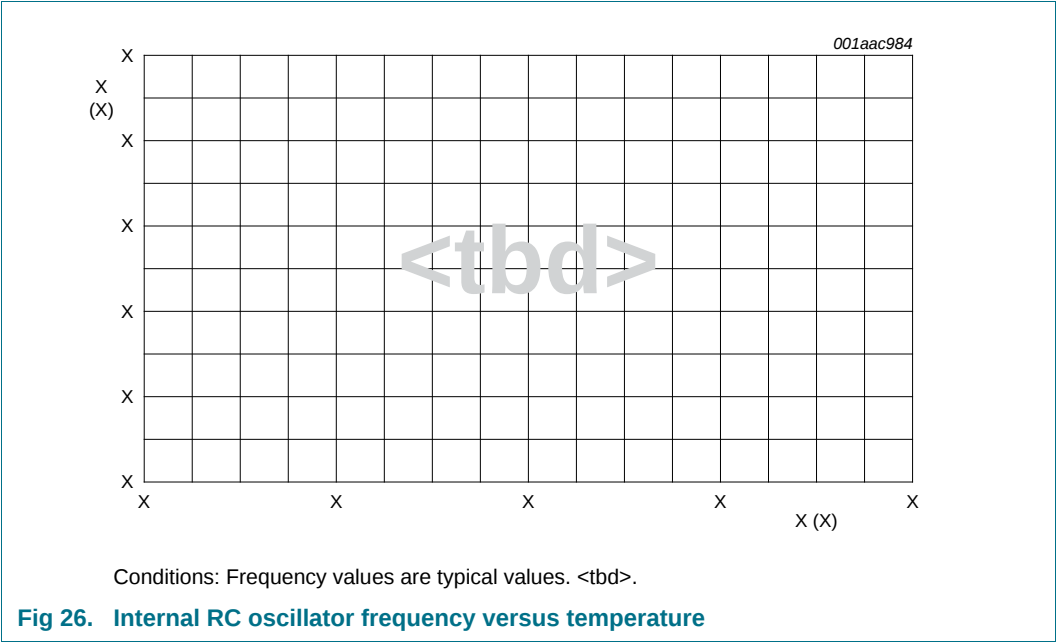


Fig 26. Internal RC oscillator frequency versus temperature

Table 14. Dynamic characteristics: Watchdog oscillator

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$f_{\text{osc(int)}}$	internal oscillator frequency	DIVSEL = 0x1F, FREQSEL = 0x1 in the WDTOSCCTRL register;	[2][3] -	9.4	-	kHz
		DIVSEL = 0x00, FREQSEL = 0xF in the WDTOSCCTRL register	[2][3] -	2300	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{\text{amb}} = -40\text{ °C}$ to $+85\text{ °C}$) is $\pm 40\%$.

[3] See the *LPC800 user manual*.

Table 15. Dynamic characteristics: Low-power oscillator

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
$f_{\text{osc(int)}}$	internal oscillator frequency		[2][3] -	9.4	-	kHz

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] The typical frequency spread over processing and temperature ($T_{\text{amb}} = -40\text{ °C}$ to $+85\text{ °C}$) is $\pm 40\%$.

[3] See the *LPC800 user manual*.

11.5 I/O pins

Table 16. Dynamic characteristics: I/O pins^[1]

$T_{\text{amb}} = -40\text{ °C}$ to $+85\text{ °C}$; $3.0\text{ V} \leq V_{\text{DD}} \leq 3.6\text{ V}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_r	rise time	pin configured as output	3.0	-	5.0	ns
t_f	fall time	pin configured as output	2.5	-	5.0	ns

[1] Applies to standard port pins and $\overline{\text{RESET}}$ pin.

11.6 I²C-bus

Table 17. Dynamic characteristic: I²C-bus pins^[1]

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.^[2]

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCL}	SCL clock frequency	Standard-mode	0	100	kHz
		Fast-mode	0	400	kHz
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	1	MHz
t_f	fall time	[4][5][6][7] of both SDA and SCL signals	-	300	ns
		Standard-mode			
		Fast-mode	$20 + 0.1 \times C_b$	300	ns
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	-	120	ns
t_{LOW}	LOW period of the SCL clock	Standard-mode	4.7	-	μs
		Fast-mode	1.3	-	μs
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.5	-	μs
t_{HIGH}	HIGH period of the SCL clock	Standard-mode	4.0	-	μs
		Fast-mode	0.6	-	μs
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	0.26	-	μs
$t_{HD;DAT}$	data hold time	[3][4][8] Standard-mode	0	-	μs
		Fast-mode	0	-	μs
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	0	-	μs
$t_{SU;DAT}$	data set-up time	[9][10] Standard-mode	250	-	ns
		Fast-mode	100	-	ns
		Fast-mode Plus; on pins PIO0_10 and PIO0_11	50	-	ns

[1] See the I²C-bus specification *UM10204* for details.

[2] Parameters are valid over operating temperature range unless otherwise specified.

[3] $t_{HD;DAT}$ is the data hold time that is measured from the falling edge of SCL; applies to data in transmission and the acknowledge.

[4] A device must internally provide a hold time of at least 300 ns for the SDA signal (with respect to the $V_{IH(min)}$ of the SCL signal) to bridge the undefined region of the falling edge of SCL.

[5] C_b = total capacitance of one bus line in pF.

[6] The maximum t_f for the SDA and SCL bus lines is specified at 300 ns. The maximum fall time for the SDA output stage t_f is specified at 250 ns. This allows series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f .

[7] In Fast-mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.

- [8] The maximum $t_{HD;DAT}$ could be 3.45 μ s and 0.9 μ s for Standard-mode and Fast-mode but must be less than the maximum of $t_{VD;DAT}$ or $t_{VD;ACK}$ by a transition time (see UM10204). This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
- [9] $t_{SU;DAT}$ is the data set-up time that is measured with respect to the rising edge of SCL; applies to data in transmission and the acknowledge.
- [10] A Fast-mode I²C-bus device can be used in a Standard-mode I²C-bus system but the requirement $t_{SU;DAT} = 250$ ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{r(max)} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

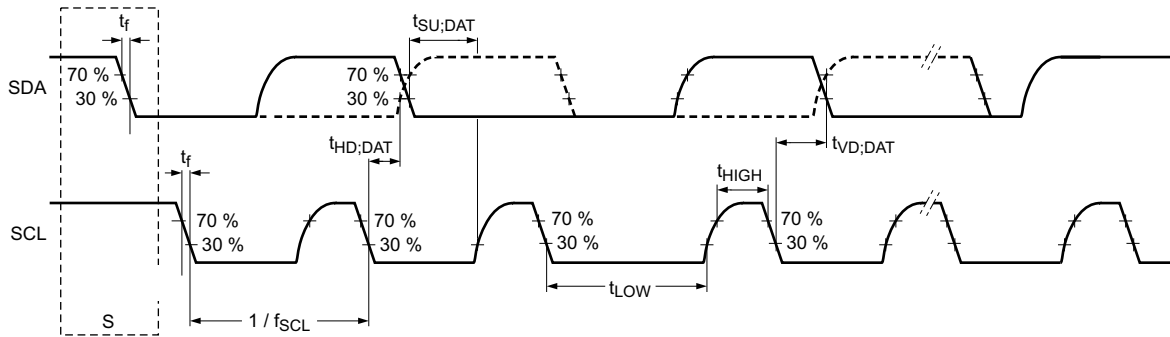


Fig 27. I²C-bus pins clock timing

11.7 SPI interfaces

The maximum data bit rate is 30 Mbit/s in slave and master modes.

Remark: SPI functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 18. Dynamic characteristics of SPI pins

$T_{amb} = -40$ °C to 85 °C; $C_L = <td>$; 1.8 V $\leq V_{DD} \leq 3.6$ V. Simulated parameters; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI master (in SPI mode)						
$T_{cy(clk)}$	clock cycle time	full-duplex mode [1]	<td>	-	-	ns
		when only transmitting [1]	<td>	-	-	ns
t_{DS}	data set-up time	in SPI mode	<td>	-	-	ns
		2.4 V $\leq V_{DD} \leq 3.6$ V	<td>	-	-	ns
		2.0 V $\leq V_{DD} < 2.4$ V	<td>	-	-	ns
		1.8 V $\leq V_{DD} < 2.0$ V	<td>	-	-	ns
t_{DH}	data hold time	in SPI mode	<td>	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	-	-	<td>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	<td>	-	-	ns

Table 18. Dynamic characteristics of SPI pins

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$; $C_L = \text{<tbid>}$; $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$. Simulated parameters; values guaranteed by design.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SPI slave (in SPI mode)						
$T_{cy(PCLK)}$	PCLK cycle time		<tbid>	-	-	ns
t_{DS}	data set-up time	in SPI mode	[2] <tbid>	-	-	ns
t_{DH}	data hold time	in SPI mode	[2] <tbid>	-	-	ns
		$2.4\text{ V} \leq V_{DD} \leq 3.6\text{ V}$				
		$2.0\text{ V} \leq V_{DD} < 2.4\text{ V}$	<tbid>			ns
		$1.8\text{ V} \leq V_{DD} < 2.0\text{ V}$	<tbid>	-	-	ns
$t_{v(Q)}$	data output valid time	in SPI mode	[2] -	-	<tbid>	ns
$t_{h(Q)}$	data output hold time	in SPI mode	[2] -	-	<tbid>	ns

[1] $T_{cy(clk)} = \text{<tbid>}$.

[2] $T_{cy(clk)} = 12 \times T_{cy(PCLK)}$.

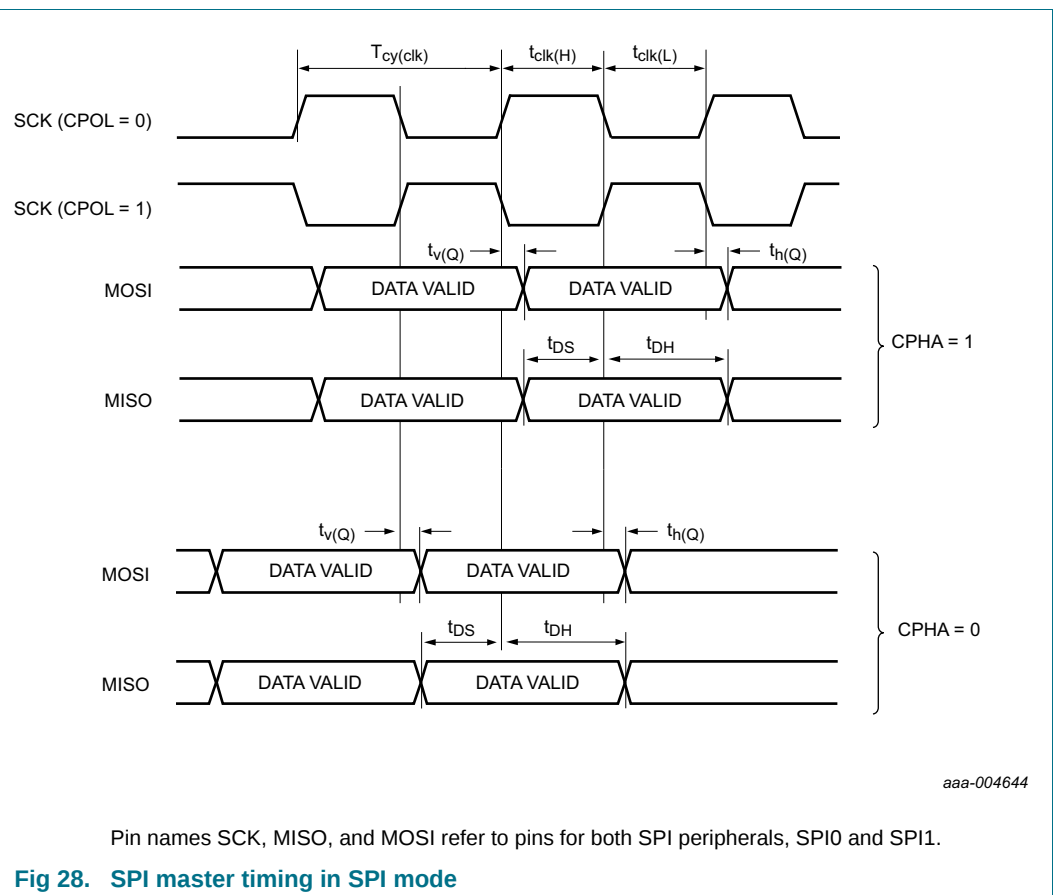
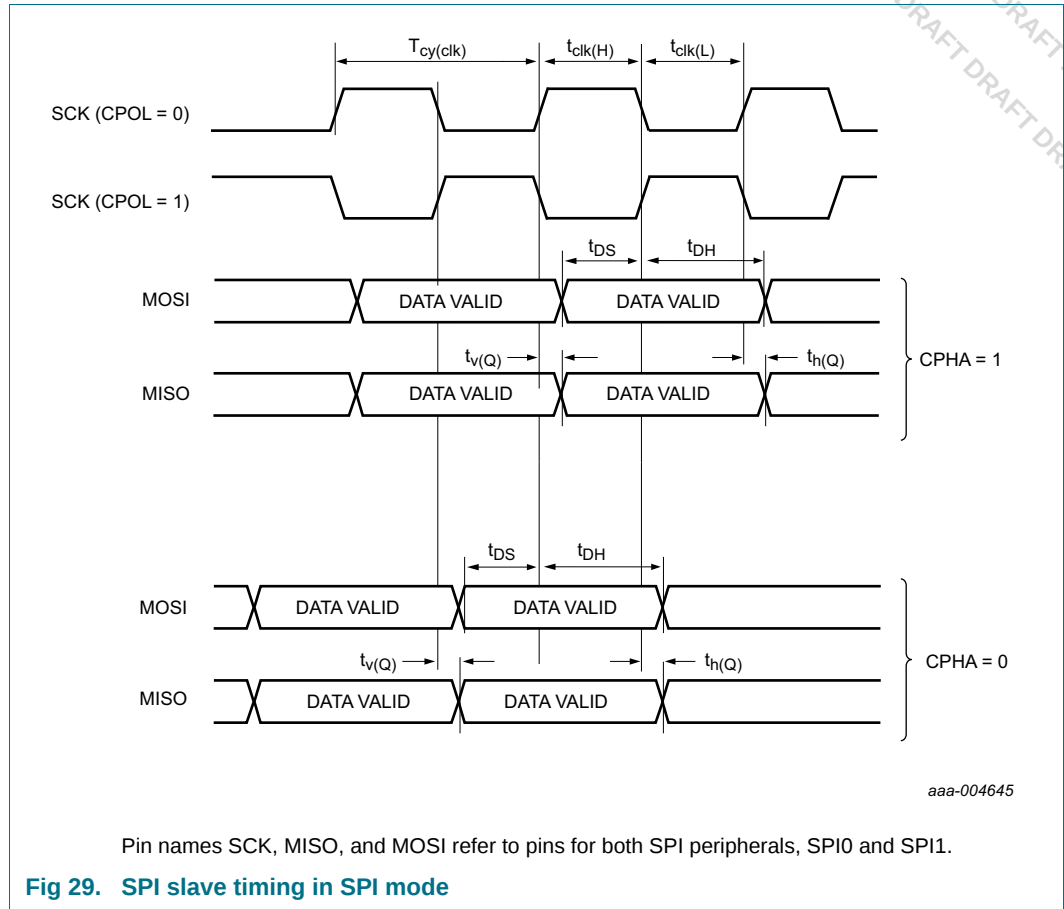


Fig 28. SPI master timing in SPI mode



11.8 USART interface

The maximum USART bit rate is 1.875 Mbit/s in asynchronous mode and 30 Mbit/s in synchronous mode slave and master mode.

Remark: USART functions can be assigned to all digital pins. The characteristics are valid for all digital pins except the open-drain pins PIO0_10 and PIO0_11.

Table 19. Dynamic characteristics: USART interface in synchronous master mode

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $85\text{ }^{\circ}\text{C}$; $1.8\text{ V} \leq V_{DD} \leq 3.6\text{ V}$; $C_L = <tb> \text{ pF}$. Simulated values.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{cy(clk)}$	clock cycle time	on pins Ux_SCLK	-	<tb>	-	μs
output						
$t_{V(Q)}$	data output valid time	on pin Ux_TXD	-	<tb>	-	ns

12. Analog characteristics

12.1 BOD

Table 20. BOD static characteristics^[1]

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}	threshold voltage	interrupt level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		interrupt level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 0				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 1				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 2				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V
		reset level 3				
		assertion	-	<tbd>	-	V
		de-assertion	-	<tbd>	-	V

[1] Interrupt levels are selected by writing the level value to the BOD control register BODCTRL.

12.2 POR

Table 21. POR static characteristics

$T_{amb} = 25\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{th}		V_{DD} rising<tbd>				
		V_{DD} falling<tbd>	-	<tbd>	-	V

12.3 Comparator

Table 22. Comparator characteristics

$V_{DD(3V3)} = 3.0\text{ V}$ and $T_{amb} = 25\text{ °C}$ unless noted otherwise.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
Static characteristics							
I _{DD}	supply current		-	<tb>	-	μA	
V _{IC}	common-mode input voltage		0	-	V _{DD}	V	
DV _O	output voltage variation		0	-	V _{DD}	V	
V _{offset}	offset voltage	V _{IC} = 0.1 V	-	<tb>	-	mV	
		V _{IC} = 1.5 V	-	<tb>	-	mV	
		V _{IC} = 2.8 V	-	<tb>	-	mV	
Dynamic characteristics							
t _{startup}	start-up time	nominal process	-	<tb>	-	μs	
t _{PD}	propagation delay	HIGH to LOW; V _{DD(3V3)} = 3.0 V; V _{IC} = 0.1 V; 50 mV overdrive input	[1]	-	<tb>	<tb>	ns
		V _{IC} = 0.1 V; rail-to-rail input	[1]	-	<tb>	<tb>	ns
		V _{IC} = 1.5 V; 50 mV overdrive input	[1]	-	<tb>	<tb>	ns
		V _{IC} = 1.5 V; rail-to-rail input	[1]	-	<tb>	<tb>	ns
		V _{IC} = 2.9 V; 50 mV overdrive input	[1]	-	<tb>	<tb>	ns
		V _{IC} = 2.9 V; rail-to-rail input	[1]	-	<tb>	<tb>	ns
		t _{PD}	propagation delay	LOW to HIGH; V _{DD(3V3)} = 3.0 V; V _{IC} = 0.1 V; 50 mV overdrive input	[1]	-	<tb>
V _{IC} = 0.1 V; rail-to-rail input	[1]			-	<tb>	<tb>	ns
V _{IC} = 1.5 V; 50 mV overdrive input	[1]			-	<tb>	<tb>	ns
V _{IC} = 1.5 V; rail-to-rail input	[1]			-	<tb>	<tb>	ns
V _{IC} = 2.9 V; 50 mV overdrive input	[1]			-	<tb>	<tb>	ns
V _{IC} = 2.9 V; rail-to-rail input	[1]			-	<tb>	<tb>	ns
V _{hys}	hysteresis voltage			positive hysteresis; V _{DD(3V3)} = 3.0 V; V _{IC} = 1.5 V	[2]	-	<tb>
V _{hys}	hysteresis voltage	negative hysteresis; V _{DD(3V3)} = 3.0 V; V _{IC} = 1.5 V	[2]	-	<tb>	-	mV
R _{lad}	ladder resistance	-	-	<tb>	-	MΩ	

[1] $C_L = 10\text{ pF}$; results from measurements on silicon samples over process corners and over the full temperature range $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$.

[2] Input hysteresis is relative to the reference input channel and is software programmable.

Table 23. Comparator voltage ladder dynamic characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{s(pu)}$	power-up settling time	to 99% of voltage ladder output value	[1]	-	<tbd>	μs
$t_{s(sw)}$	switching settling time	to 99% of voltage ladder output value	[1]	-	<tbd>	μs
			[2]	-	<tbd>	

- [1] Maximum values are derived from worst case simulation ($V_{DD} = 2.6\text{ V}$; $T_{amb} = 85\text{ }^{\circ}\text{C}$; slow process models).
 [2] Settling time applies to switching between comparator channels<tb>.

Table 24. Comparator voltage ladder reference static characteristics

$V_{DD(3V3)} = 3.3\text{ V}$; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$.

Symbol	Parameter	Conditions	Min	Typ	Max ^[1]	Unit
$E_{V(O)}$	output voltage error	Internal $V_{DD(3V3)}$ supply		<tb>	<tb>	
		decimal code = 00 ^[2]	-			%
		decimal code = 08	-	<tb>	<tb>	%
		decimal code = 16	-	<tb>	<tb>	%
		decimal code = 24	-	<tb>	<tb>	%
		decimal code = 30	-	<tb>	<tb>	%
$E_{V(O)}$	output voltage error	External V_{DDCMP} supply		<tb>	<tb>	
		decimal code = 00	-			%
		decimal code = 08	-	<tb>	<tb>	%
		decimal code = 16	-	<tb>	<tb>	%
		decimal code = 24	-	<tb>	<tb>	%
		decimal code = 30	-	<tb>	<tb>	%

- [1] Measured <tb> with a 2 kHz input signal and overdrive < 100 μV .
 [2] All peripherals except comparator, temperature sensor, and IRC turned off.

13. Application information

13.1 XTAL input

The input voltage to the on-chip oscillators is limited to 1.8 V. If the oscillator is driven by a clock in slave mode, it is recommended that the input be coupled through a capacitor with $C_i = 100\text{ pF}$. To limit the input voltage to the specified range, choose an additional capacitor to ground C_g which attenuates the input voltage by a factor $C_i/(C_i + C_g)$. In slave mode, a minimum of 200 mV(RMS) is needed.

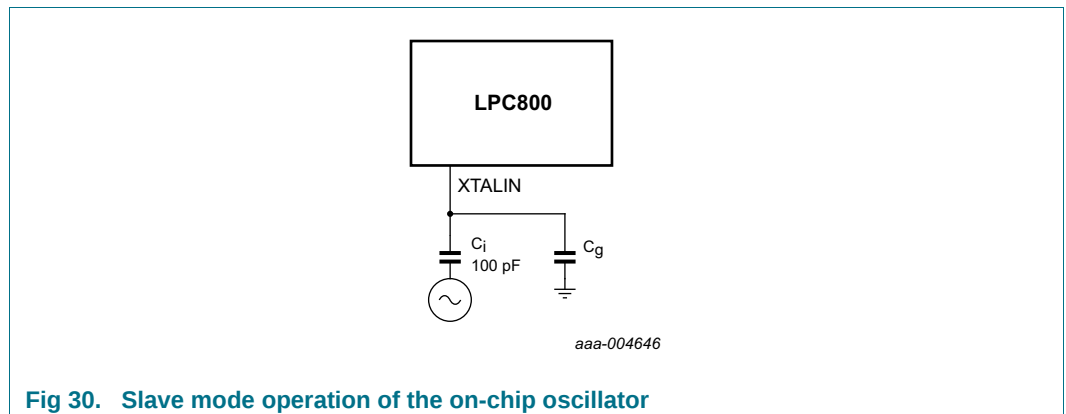


Fig 30. Slave mode operation of the on-chip oscillator

In slave mode the input clock signal should be coupled by means of a capacitor of 100 pF (Figure 30), with an amplitude between 200 mV (RMS) and 1000 mV (RMS). This corresponds to a square wave signal with a signal swing of between 280 mV and 1.4 V. The XTALOUT pin in this configuration can be left unconnected.

External components and models used in oscillation mode are shown in Figure 31 and in Table 25 and Table 26. Since the feedback resistance is integrated on chip, only a crystal and the capacitances C_{X1} and C_{X2} need to be connected externally in case of fundamental mode oscillation (the fundamental frequency is represented by L , C_L and R_S). Capacitance C_P in Figure 31 represents the parallel package capacitance and should not be larger than 7 pF. Parameters F_{OSC} , C_L , R_S and C_P are supplied by the crystal manufacturer (see Table 25).

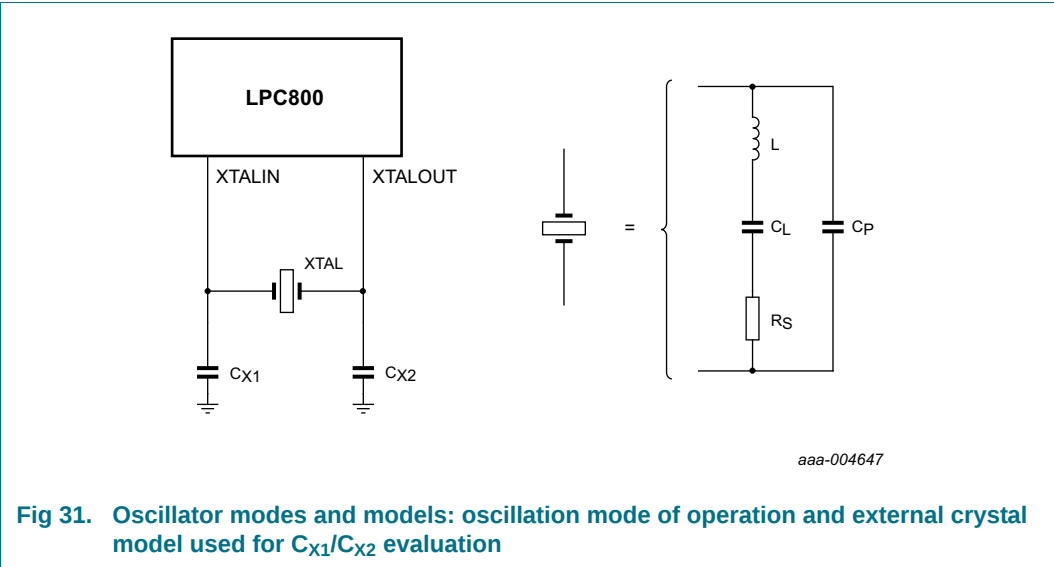


Fig 31. Oscillator modes and models: oscillation mode of operation and external crystal model used for C_{X1}/C_{X2} evaluation

Table 25. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) low frequency mode

Fundamental oscillation frequency F_{OSC}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1} , C_{X2}
1 MHz - 5 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 300 Ω	39 pF, 39 pF
	30 pF	< 300 Ω	57 pF, 57 pF
5 MHz - 10 MHz	10 pF	< 300 Ω	18 pF, 18 pF
	20 pF	< 200 Ω	39 pF, 39 pF
	30 pF	< 100 Ω	57 pF, 57 pF
10 MHz - 15 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 60 Ω	39 pF, 39 pF
15 MHz - 20 MHz	10 pF	< 80 Ω	18 pF, 18 pF

Table 26. Recommended values for C_{X1}/C_{X2} in oscillation mode (crystal and external components parameters) high frequency mode

Fundamental oscillation frequency F_{osc}	Crystal load capacitance C_L	Maximum crystal series resistance R_S	External load capacitors C_{X1}, C_{X2}
15 MHz - 20 MHz	10 pF	< 180 Ω	18 pF, 18 pF
	20 pF	< 100 Ω	39 pF, 39 pF
20 MHz - 25 MHz	10 pF	< 160 Ω	18 pF, 18 pF
	20 pF	< 80 Ω	39 pF, 39 pF

13.2 XTAL Printed Circuit Board (PCB) layout guidelines

The crystal should be connected on the PCB as close as possible to the oscillator input and output pins of the chip. Take care that the load capacitors C_{X1} , C_{X2} , and C_{X3} in case of third overtone crystal usage have a common ground plane. The external components must also be connected to the ground plain. Loops must be made as small as possible in order to keep the noise coupled in via the PCB as small as possible. Also parasitics should stay as small as possible. Values of C_{X1} and C_{X2} should be chosen smaller accordingly to the increase in parasitics of the PCB layout.

13.3 ElectroMagnetic Compatibility (EMC)

Radiated emission measurements according to the IEC61967-2 standard using the TEM-cell method are shown for the LPC800 in [Table 27](#).

Table 27. ElectroMagnetic Compatibility (EMC) for part LPC800 (TEM-cell method)
 $V_{DD} = 3.3 \text{ V}$; $T_{amb} = 25 \text{ }^{\circ}\text{C}$.

Parameter	Frequency band	System clock =			Unit
		12 MHz	24 MHz	48 MHz	
Input clock: IRC (12 MHz)					
maximum peak level	150 kHz to 30 MHz	<td>	<td>	<td>	dBμV
	30 MHz to 150 MHz	<td>	<td>	<td>	dBμV
	150 MHz to 1 GHz	<td>	<td>	<td>	dBμV
IEC level ^[1]	-	<td>	<td>	<td>	-
Input clock: crystal oscillator (12 MHz)					
maximum peak level	150 kHz to 30 MHz	<td>	<td>	<td>	dBμV
	30 MHz to 150 MHz	<td>	<td>	<td>	dBμV
	150 MHz to 1 GHz	<td>	<td>	<td>	dBμV
IEC level ^[1]	-	<td>	<td>	<td>	-

[1] IEC levels refer to Appendix D in the IEC61967-2 Specification.

14. Package outline

DIP8: plastic dual in-line package; 8 leads (300 mil) SOT97-2

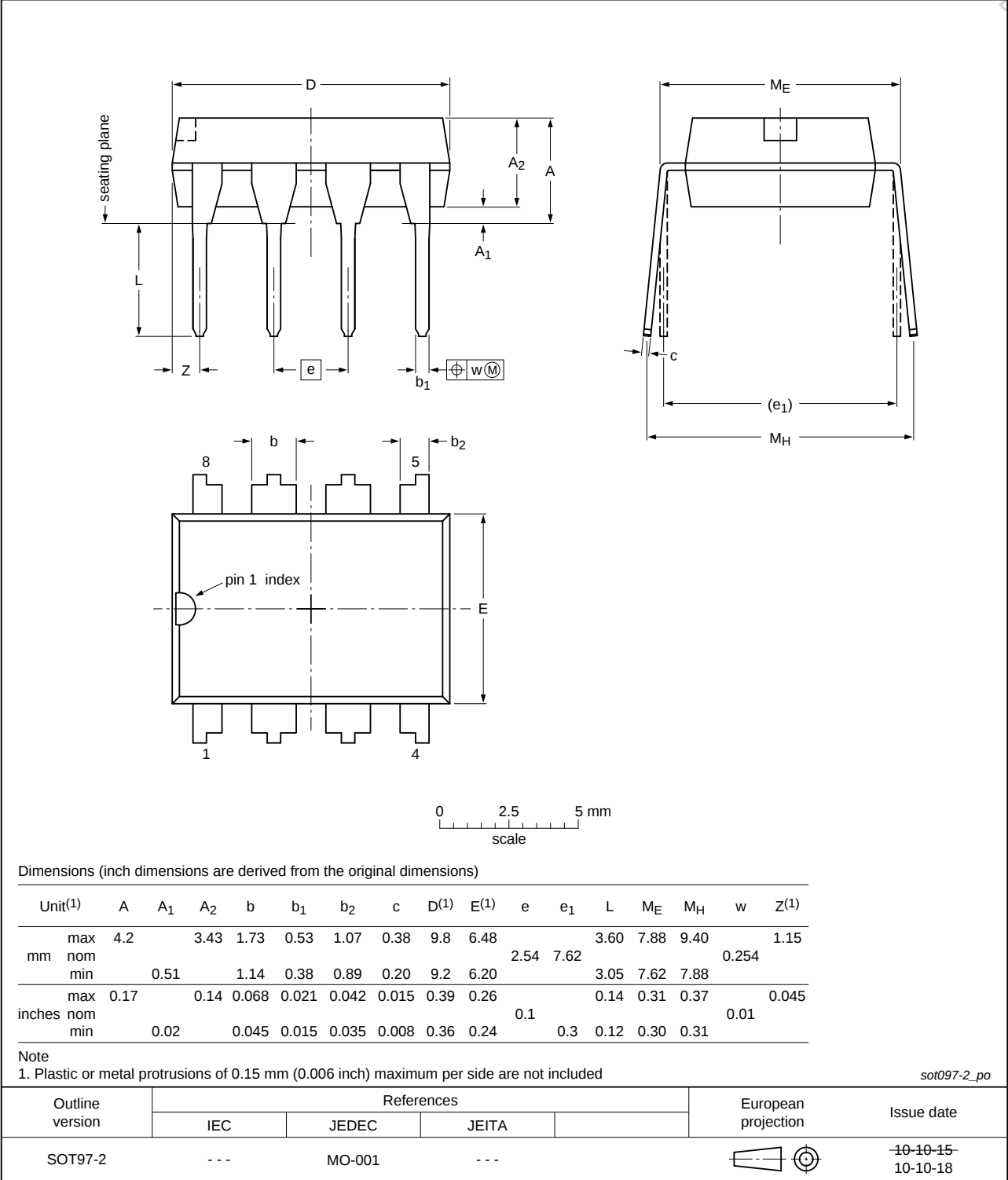


Fig 32. Package outline SOT097-2 (DIP8)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

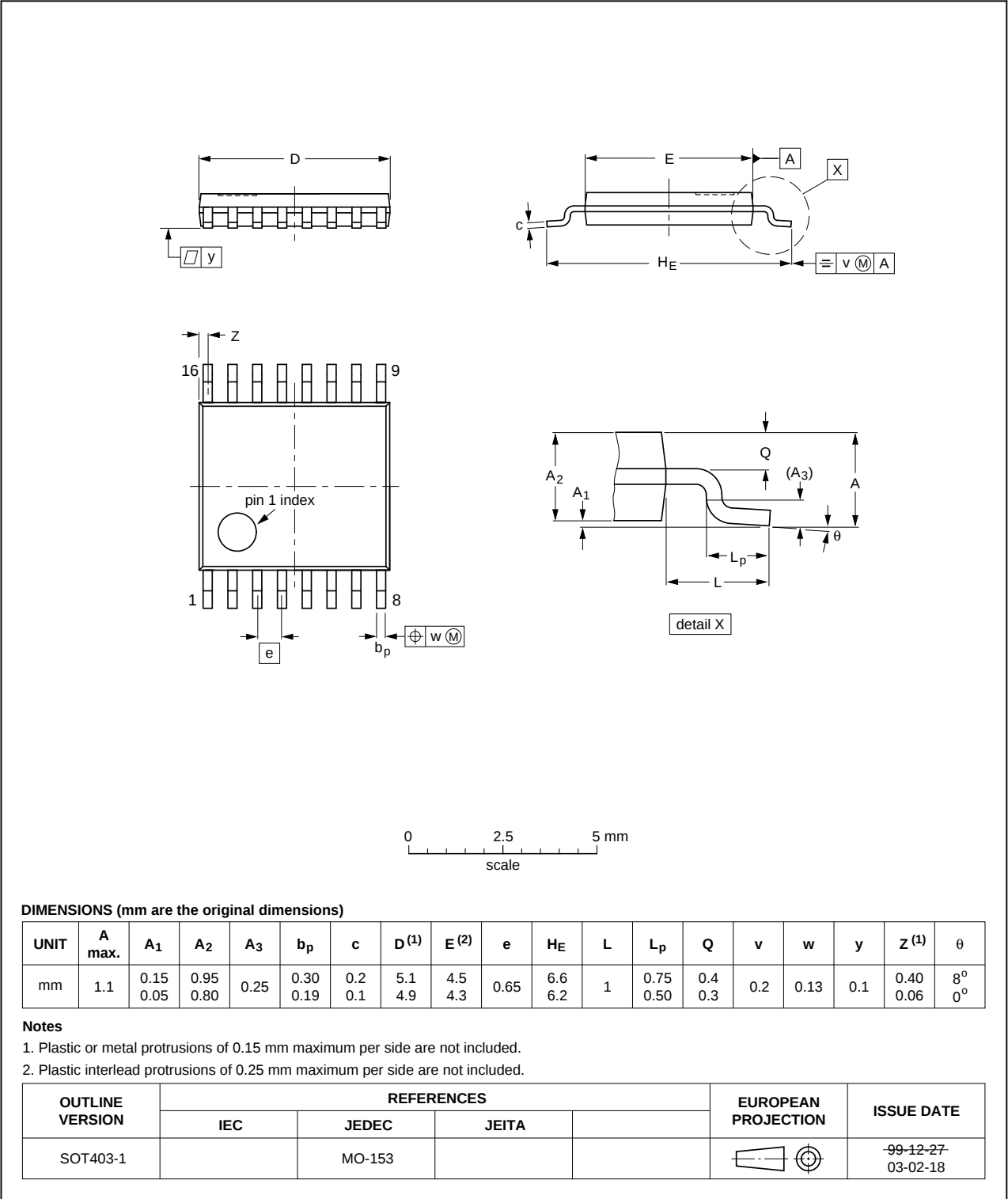


Fig 33. Package outline SOT403-1 (TSSOP16)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

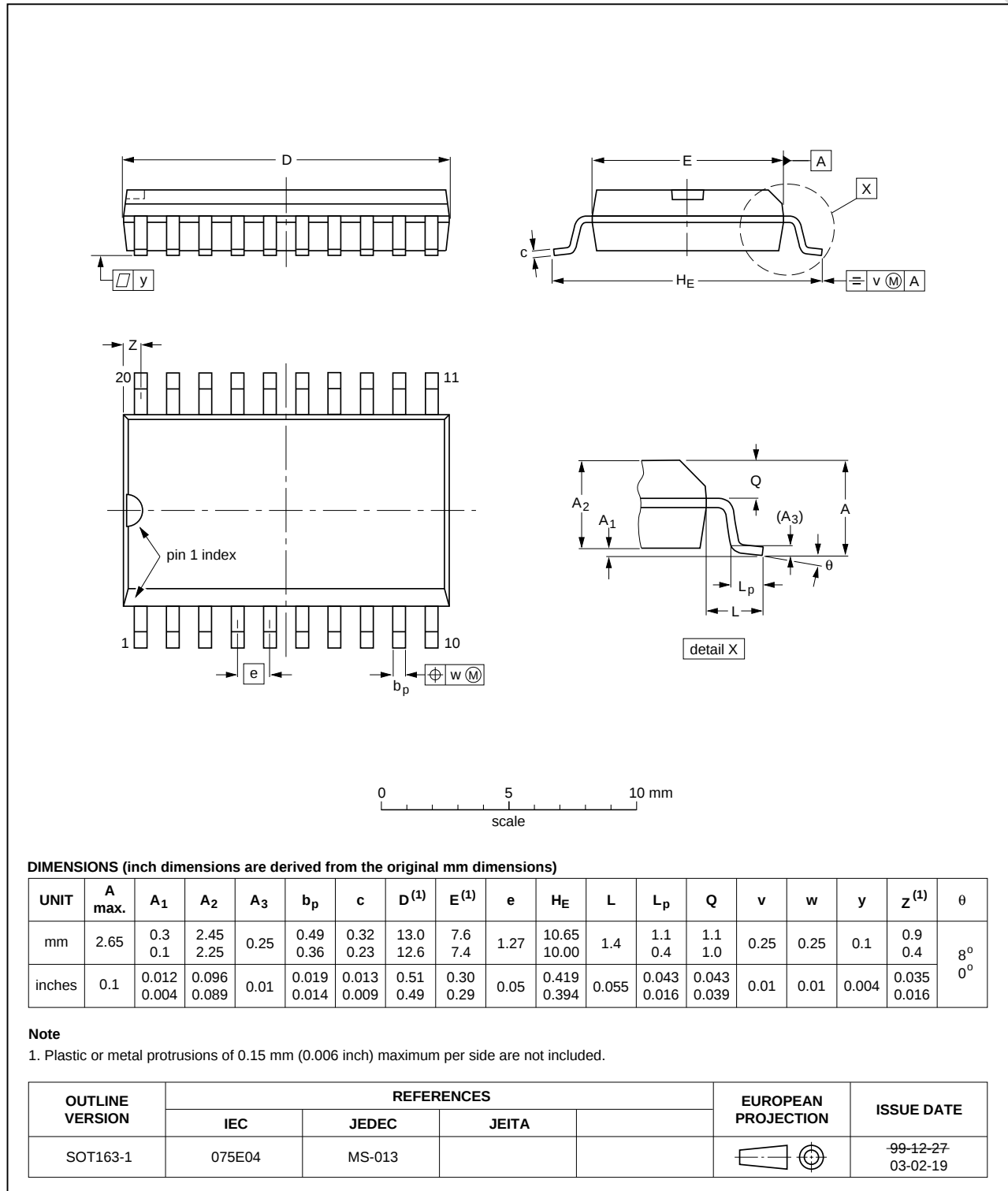


Fig 34. Package outline SOT163-1 (SO20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

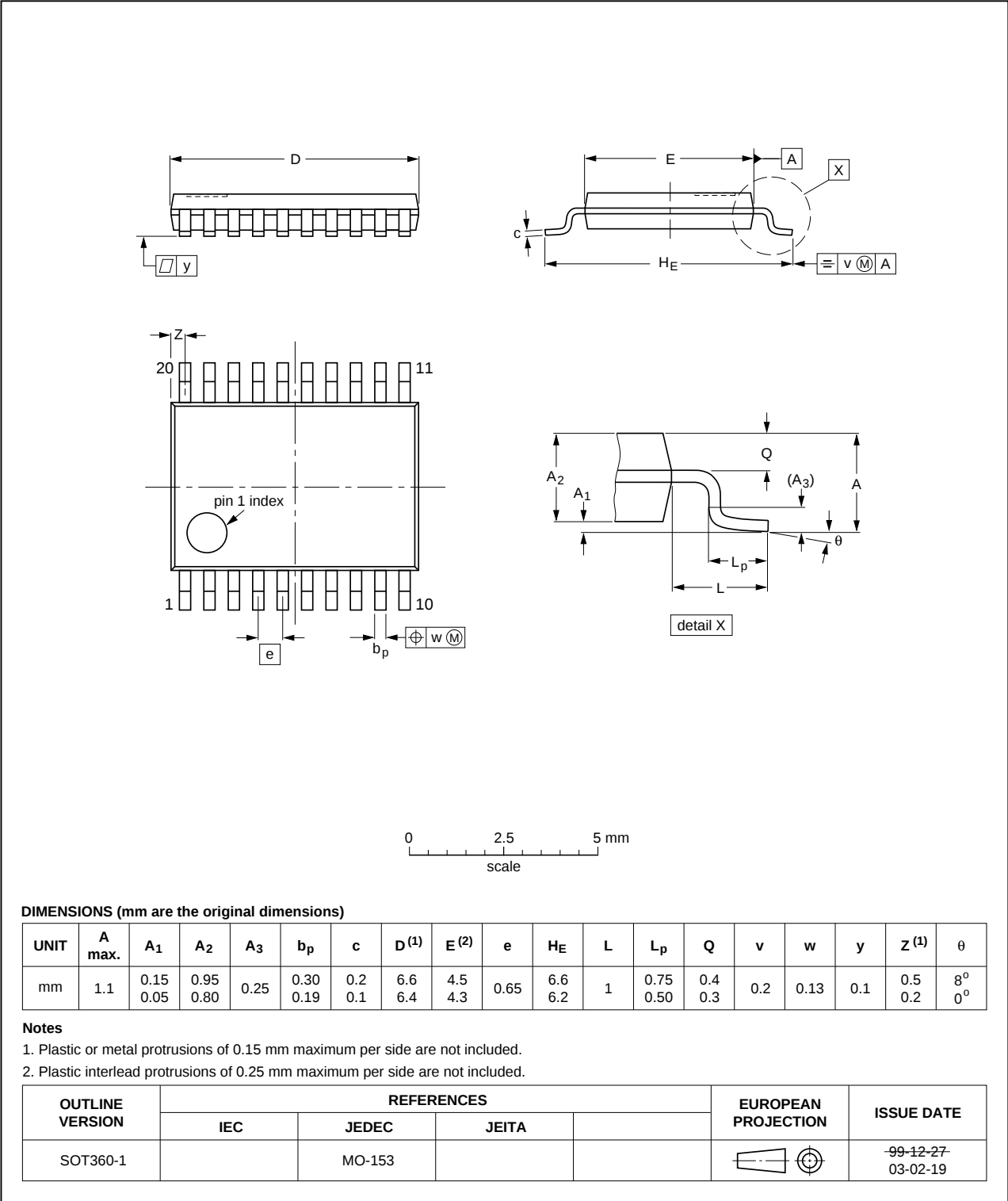


Fig 35. Package outline SOT360-1 (TSSOP20)

15. Soldering

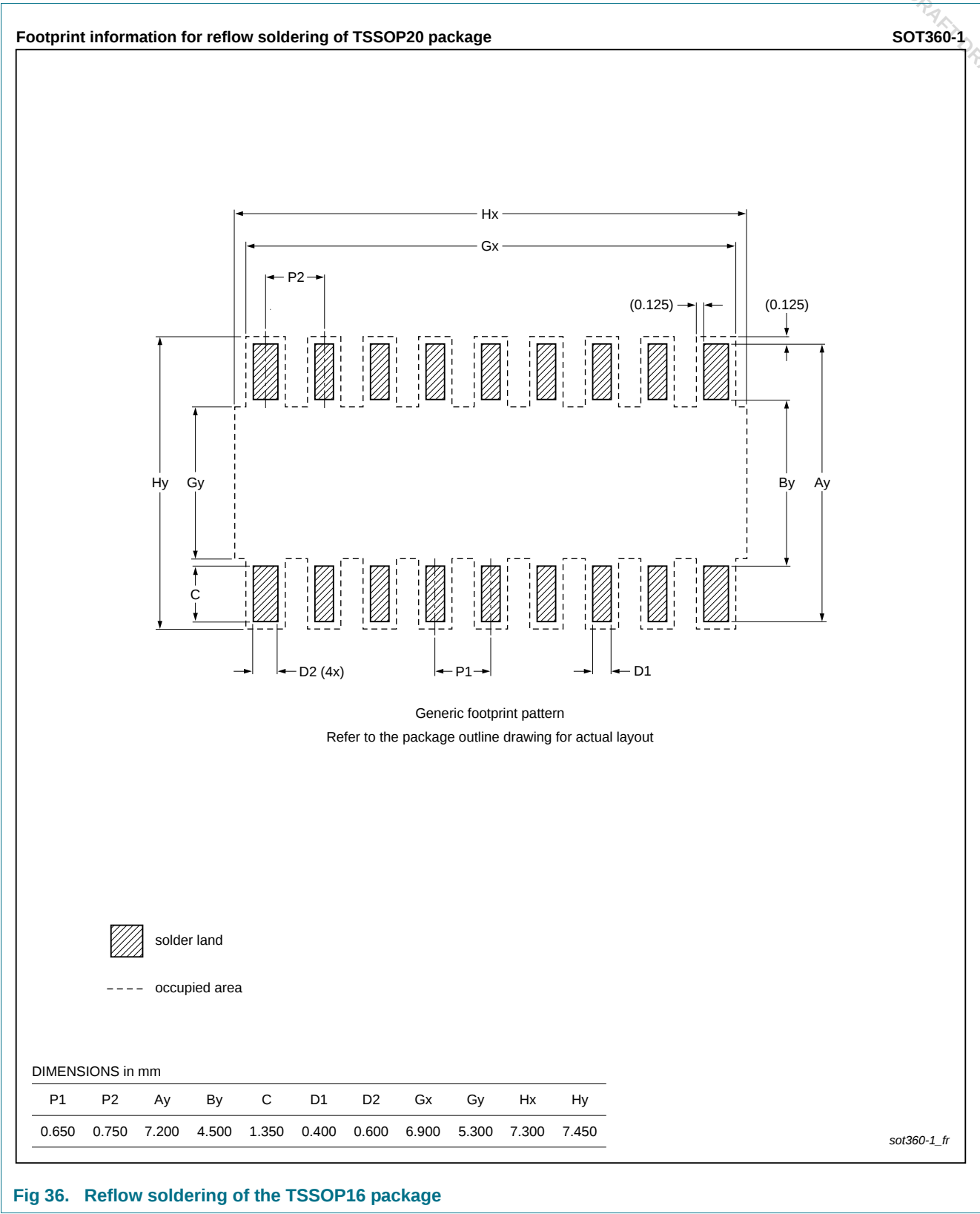


Fig 36. Reflow soldering of the TSSOP16 package

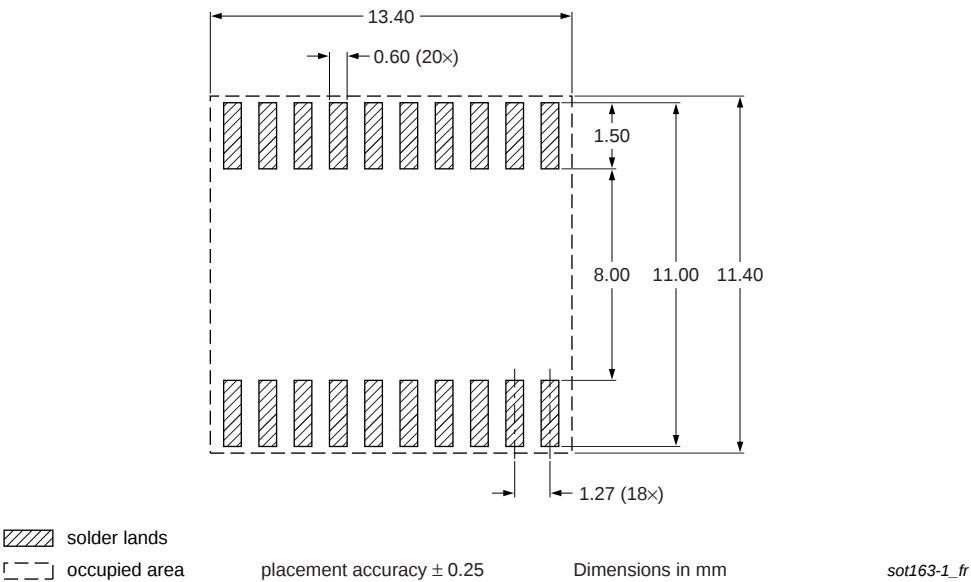


Fig 37. Reflow soldering of the SO20 package

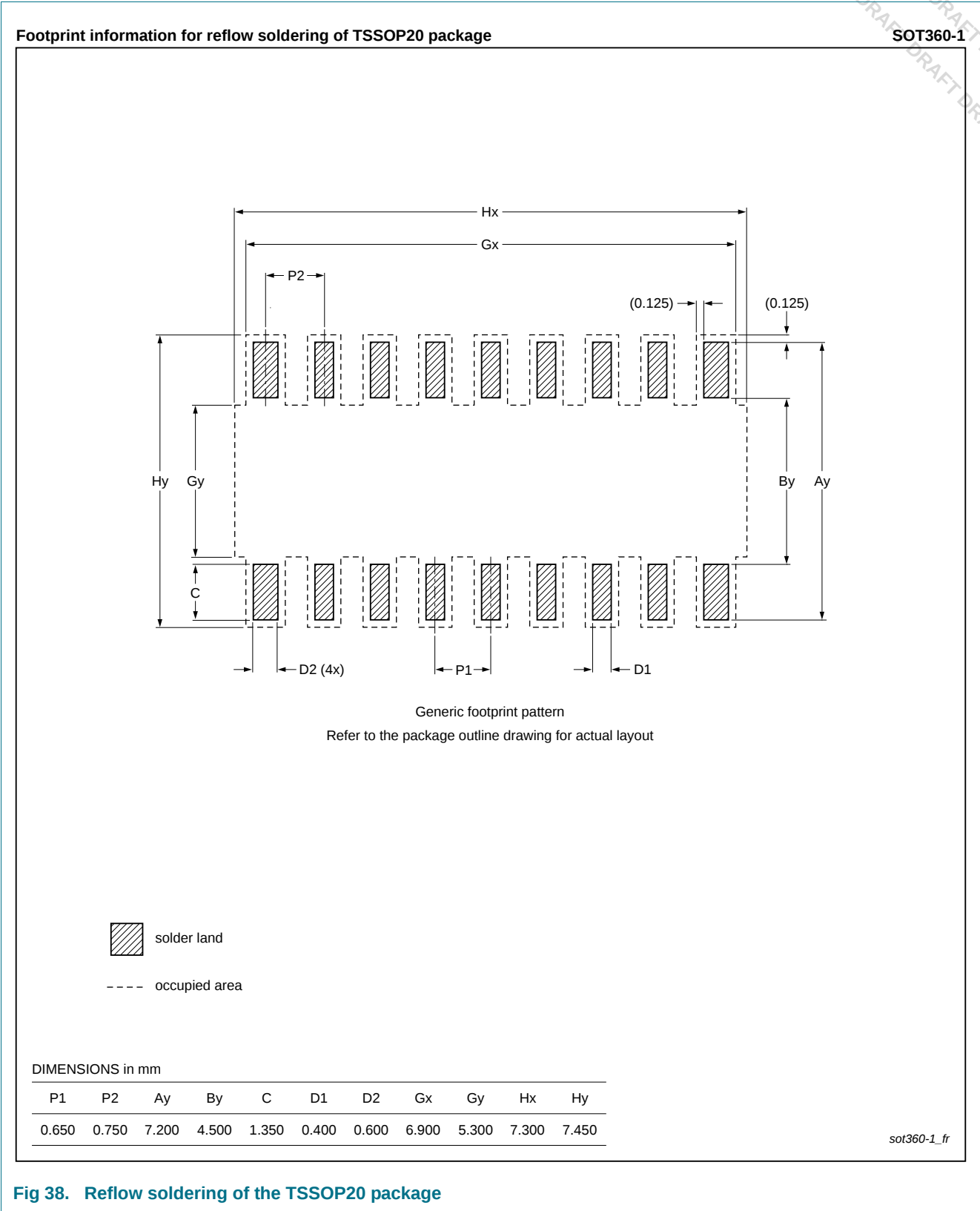


Fig 38. Reflow soldering of the TSSOP20 package

16. Abbreviations

Table 28. Abbreviations

Acronym	Description
AHB	Advanced High-performance Bus
APB	Advanced Peripheral Bus
BOD	BrownOut Detection
GPIO	General-Purpose Input/Output
PLL	Phase-Locked Loop
RC	Resistor-Capacitor
SPI	Serial Peripheral Interface
SMBus	System Management Bus
TEM	Transverse ElectroMagnetic
UART	Universal Asynchronous Receiver/Transmitter

17. References

- [1] I2C-bus specification *UM10204*.

18. Revision history

Table 29. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
LPC81xM v.1	<tbd>	Objective data sheet	-	-

19. Legal information

19.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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